BittWare a molex company | Achronix Data Acceleration


# S7t-VG6 | VectorPath™ Accelerator Card

Build your application on the latest 7nm FPGA technology

High-Performance
- Compute
- Data Delivery

Advanced FPGA acceleration performance is not just about adding gates, it is about better high-bandwidth routing for data, more tailored programmable elements, higher-bandwidth large memory blocks and next-generation networking support.

Introducing the **S7t VectorPath** accelerator card from **BittWare**, featuring the **Achronix® 7nm Speedster®7t FPGA**. Explore the features that can give your application next-generation acceleration in both compute and data delivery.

## Application Areas

### Compute

**Designed for compute-intensive applications**

- 8× GDDR6 memories delivering 3.5Tbps of aggregate bandwidth
- Machine learning processors (MLP) optimized for AI/ML functionality:
  - Support for BFP, FP and INT numerical formats
  - Co-located memory for reduced latency
  - Direct connect to two-dimensional (2D) network on chip (NoC)


### Network

**QSFP-DD and QSFP56 ports cater to a wide range of high-speed networking applications**

- Hard multi-rate MAC for 10-400 GbE
- 2D NoC delivering >20 Tbps bandwidth for data streaming, both on and off chip

### Storage

**NVMe access for data recorder and data processing applications**

- MCIO expansion to NVMe flash
- Stream directly from network ports to flash arrays

### Sensor Processing

**Optimize for your specific application requirements using GPIO and SerDes expansion ports**

- Directly interface to custom data and control signals
- Directly-attach to complementary sensor and processor technologies

# Speedster7t FPGA

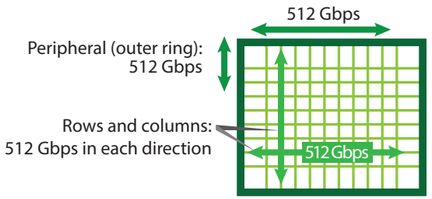
## Revolutionary Chip Design by Achronix

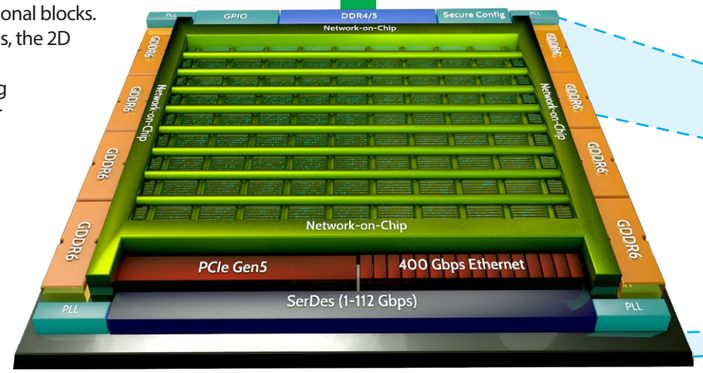
Unlocking the potential of TSMC's **7nm** FinFET technology, the Speedster7t FPGA is highly optimized for AI/ML and high-bandwidth data acceleration. A Speedster7t FPGA is at the heart of every S7t accelerator card.

## 2D NoC — Two-Dimensional Network-on-Chip

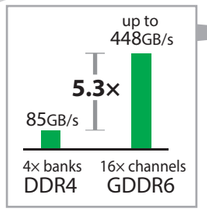
### Data Highway Unclogs FPGA Fabric

The 2D NoC is the Speedster7t FPGA's super highway moving data at high speed interconnecting edge subsystems such as GDDR6, DDR4, DDR5, Ethernet and PCI-e as well as internal FPGA functional blocks. Made up of an outer ring and a grid of rows and columns, the 2D NoC connects external and internal interfaces with an aggregated bandwidth exceeding 20Tbps without using FPGA fabric resources, for example, the host can transfer data to GDDR6 through PCIe.




## GDDR6 Memory




### 6× Faster Large Memory

Using high-bandwidth GDDR6 memory, the S7t gives your application a large memory resource of 16 Gigabytes, but at more than 5 times greater bandwidth.

Plus with the 2D NoC, the GDDR6 is available for read/write from the host over PCIe without using FPGA resources.

## Up to 400GbE Networking

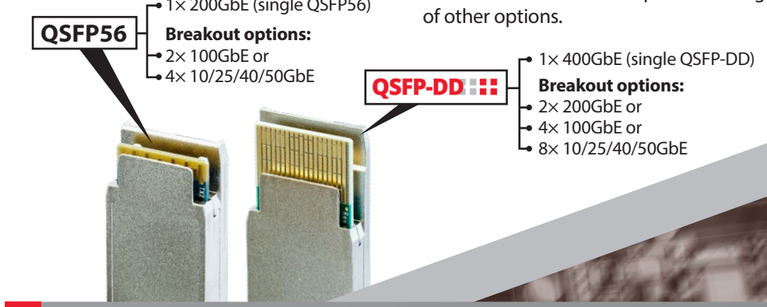
The S7t card offers a range of network interfaces connected to the Speedster7t FPGA fabric. The card supports 56G PAM4, with hard IP MAC and FEC support. On-board jitter cleaners are available for synchronous ethernet (SyncE).

**QSFP 56G (PAM4) Interfaces**

The first interface is a QSFP56 with 4 SerDes lanes supporting up to 200GbE.

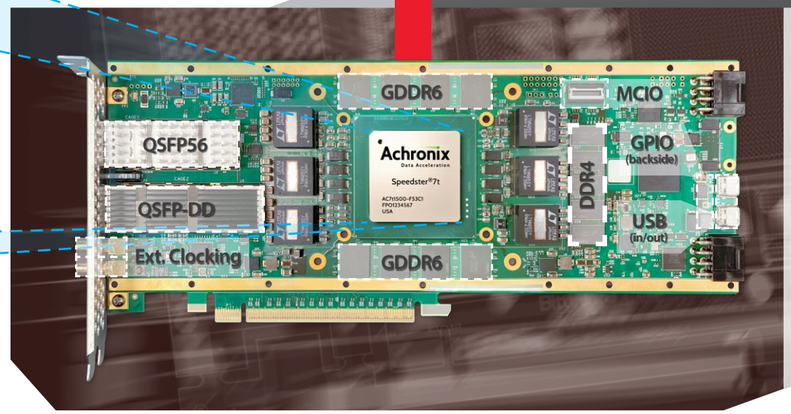
A second interface is a QSFP-DD with 8 SerDes lanes supporting up to 400GbE.

Breakout cables as shown provide a range of other options.




# S7t-*VG6* FPGA Card

## Enterprise-Class Design by BittWare




Unlocking the Speedster7t FPGA's potential is BittWare's S7t FPGA card, designed for both development and at-scale deployment.

The S7t FPGA card delivers a wide range of advanced I/O, including 400G and multiple PCIe interfaces and the high-bandwidth GDDR6 memory.

Customers can get started quickly with the BittWare SDK, including an example project, for Linux and Windows.

## FPGA Fabric | Up to 86 Tera-Operations Per Second, 750 MHz FMax

### RLB — Reconfigurable Logic Block

The Speedster7t features RLBs: a new reconfigurable logic architecture with 6-input LUTs, 8-bit ALUs, 2 flip-flops per LUT, plus a reformulated multiplier LUT (MLUT) mode based on a modified Booth algorithm which doubles the performance of LUT-based multiplication.

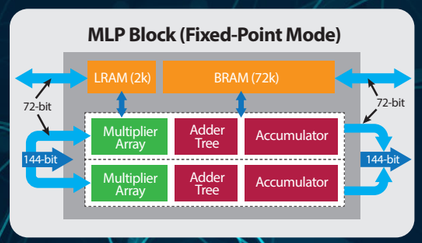
The Speedster7t ACt1500 FPGA has 692K LUTs.

### MLP — Machine Learning Processor

MLP blocks are large-scale matrix-vector and matrix-matrix multiplication engines supporting fixed- and floating-point computations. For integer multiplication, the MLP offers 4× int16, 16× int8 or 32× int4 modes. For floating point and block floating point operations, the MLP supports fp15, fp24 or bf16.

MLP blocks include two memory blocks that can be used individually or with multipliers. Total embedded memory is 190 Mb.

Total MLP blocks: 2,560 capable of 41k INT8 operations.




## PCIe, Expansion and Customization

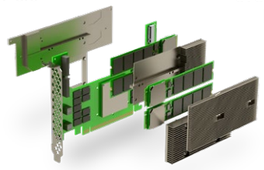
**PCIe Gen5 ×16 Interface**

The S7t card provides a PCIe Gen5 ×16 interface, directly connected to the FPGA. The BittWare SDK provides an example project including support for PCIe interaction.

**MCIO Interface with PCIe Gen5**

A 4× MCIO connector interfaces directly with a PCIe interface subsystem (inside the FPGA) for data rates up to PCIe Gen5. Example uses:

- NVMe PCIe Gen5
- Board-to-board interconnect
- Connect to accessory boards for customization options

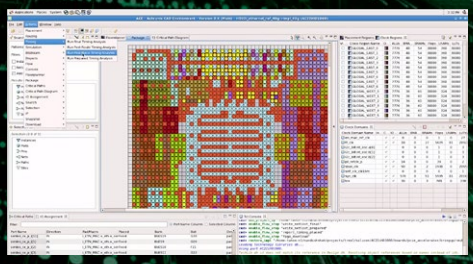


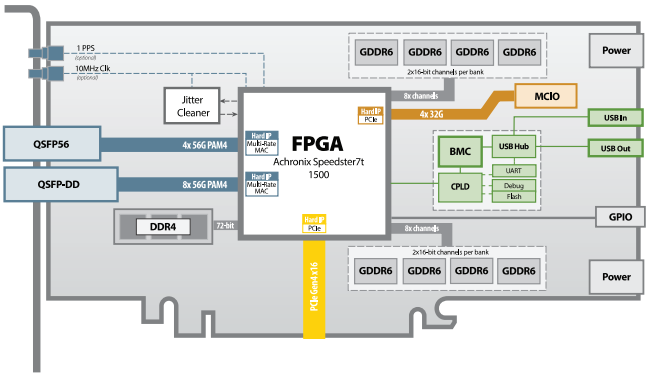
**Customization**

Thanks to three decades of building customized solutions, BittWare is your partner for everything from a simple accessory board to complete custom variations with complex mechanical requirements. Our resources include the global Molex group to handle any size project.

# ACE FPGA Development Software

The ACE software from Achronix is the development environment for the Speedster7t FPGA. ACE handles the hardware design workflow, supporting RTL (VHDL and Verilog) input together with industry-standard simulation. ACE also enables using advanced chip features such as the NoC. ACE also ship with an Achronix-optimized version of Synplify Pro from Synopsys.






## Additional Card Features

- Jitter cleaner for SyncE
- Front-panel 1 PPS & ext. ref. clock
- BMC with health monitoring
- 8× GPIO pins
- Drivers for Linux and Windows

## Software Development Kit: Powerful Tools for Development

The BittWare Software Development Kit (SDK) provides drivers, libraries, utilities and an example project for accessing, integrating and developing applications for the S7t.

## TeraBox Development Platform Available

Let us handle the server integration and start your application proof-of-concept without having to dedicate additional valuable resources for setup!

## Extend your warranty with TeraBox

By purchasing cards in most TeraBox servers, you extend the warranty to three years. Ask us for details when you get a price quote.

## Card Specifications

| | |
|---|---|
| FPGA | • Achronix Speedster AC7t1500<br>  • 52.5 x52.5 package<br>  • 692K 6-input lookup tables (LUTs)<br>  • 189 Mb embedded RAM<br>  • 2,560 MLPs |
| On-board memory | • 16 GBytes GDDR6: 8 banks (2 independant 16-bit, 14 Gbps channels per bank), 3.5 Tbps aggregate b/w<br>• One bank DDR4-2666 with ECC, 4 GBytes (x72)<br>• Flash memory for booting FPGA |
| Host interface | • PCIe Gen5 x16 host interface |
| External clocking | • 1 PPS and 10MHz ref clk front panel inputs |
| USB | • USB port for access to BMC, USB-JTAG, USB-UART<br>• Additional USB port for daisy chain |
| MCIO | • MCIO connected to FPGA via 4x transceivers<br>• PCIe Gen5 Hard IP |
| GPIO | • 8 GPIO pins, 3.3V, single ended, direction (Tx, Rx) independently settable by FPGA per GPIO, buffers rated to 200Mbps |
| QSFP cages | • QSFP-DD cage on front panel<br>  • 56G PAM4 transceivers<br>  • 1x 400GbE, 4x 100GbE, or 8x 10/25/40/50 GbE<br>  • Hard MAC and FEC for every speed<br>• QSFP56 cage on front panel<br>  • 56G PAM4 transceivers<br>  • 2x 100GbE or 4x 10/25/40/50 GbE<br>  • Hard MAC and FEC every speed |
| Board Management Controller | • Voltage, current, temperature monitoring<br>• Power sequencing and reset<br>• Field upgrades<br>• FPGA configuration and control<br>• Clock configuration<br>• I²C bus access<br>• USB 2.0<br>• Voltage overrides |
| Cooling | • Standard: dual-width passive heatsink<br>• Optional: dual-width active heatsink<br>• Optional: dual-width liquid cooling |
| Electrical | • On-board power from two AUX connectors (8-pin)<br>• Power dissipation is application dependent<br>• Typical max power consumption TBD |
| Environmental | • Operating temperature 5°C to 35°C<br>• Airflow requirements: contact BittWare |
| Form factor | • Standard-height PCIe dual-width board<br>• Size: 111.15mm x 266.70mm (4.376in x 10.500in) |

## Development Tools

| | |
|---|---|
| System development | • Software development toolkit including PCIe driver, libraries, and board monitoring utilities |
| FPGA development | • Achronix tools—ACE Design Tools<br>• FPGA example projects |

**For more pricing or more information, visit BittWare.com/S7t-VG6**

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