S7t-VG6 VectorPath™ Accelerator Card

Build your application on the latest 7nm FPGA technology

Advancing FPGA acceleration performance isn’t just about adding gates, it’s about better highways for data, more tailored programmable elements, higher-bandwidth large memory and next-generation networking support.

Introducing the S7t VectorPath accelerator card from BittWare, featuring the Achronix® 7nm Speedster® 7t FPGA. Explore the features that can give your application next-generation acceleration in both compute and data delivery.

Application Areas

Compute
Designed to address the most demanding compute-intensive applications
- 8x GDDR6 memories delivering 4Tbps of aggregate bandwidth
- Machine Learning Processors (MLP) optimized for AI/ML functionality:
  - Up to 41K INT8 MACs and 134 INT4 TOPS
- Multiple floating-point and integer numerical formats

Network
QSFP-DD and QSFP56 ports cater to a wide range of high-speed network applications
- Hardened Multi-rate MAC for 10-400 GbE
- Network-on-Chip (NoC) delivers 20Tbps bandwidth for data to stream in, out and across the device

Storage
NVMe access for data recorder and data processing applications
- OCuLink expansion to NVMe flash
- Stream directly from network ports to flash arrays

Sensor Processing
Optimize for your specific application requirements using GPIO and SerDes expansion ports
- Directly interface to custom data and control signals
- Directly-attach to complementary sensor and processor technologies
Unlocking the potential of TSMC’s 7nm FinFET technology, the Speedster7t FPGA is highly optimized for AI/ML and high-bandwidth data acceleration. It’s at the heart of every S7t accelerator card.

Unlocking the Speedster7t FPGA’s potential is BittWare’s S7t FPGA card, designed for both development and scale deployment. We’ve given users a wide range of advanced I/O, including 400G and multiple PCIe interfaces and the high-bandwidth GDDR6 memory. Customers can get started quickly with the BittWorks II Toolkit, including example projects, for Linux and Windows.

The Speedster7t features RLBs: a new reconfigurable logic architecture with 6-input LUTs, 8-bit ALUs, 2 flip-flops per LUT and a reconfigured multiplier LUT (MLUT) model based on a modified Booth algorithm which doubles the performance of LUT-based multiplication. The Speedster7t FPGA has 692K LUTs.

MLP blocks are large-scale matrix-vector and matrix-matrix multiplication engines supporting fixed- and floating-point computations. The MLP offers features including integer multiply with optional accumulate, bfloat16 operations, floating point 16, block floating point and floating point 24. MLP blocks include two memory blocks that can be specified individually or with multipliers. Total embedded memory is 190 Mb. Total MLP blocks: 2,560 capable of 41k INT8 operations.

The S7t card offers a range of network interfaces connected to the Speedster7t FPGA fabric. The card supports S6G PAM4, with Hard IP MAC and FEC support. On-board jitter cleaners are available for Synchronous Ethernet.

The first interface is a QSFP56 with 4 SerDes lanes supporting up to 200GbE. A second interface is a QSFP-DD with 8 SerDes lanes supporting up to 400GbE. Breakout cables as shown provide a range of other options.

Up to 400G Networking

QSFP 56G (PAM4) Interfaces

- 1× 200GbE (single QSFP56)
- Breakout options:
  - 2× 100GbE or
  - 4× 25GbE or
  - 8× 10/25/40/50GbE

QSFP-DD

- 1× 400GbE (single QSFP-DD)
- Breakout options:
  - 2× 200GbE or
  - 4× 100GbE or
  - 8× 10/25/40/50GbE

OCuLink Interface with PCIe Gen4

- NVMe PCIe Gen4
- Board-to-board interconnect
- Connect to accessory boards for customization options

Customization

Thanks to three decades of building customized solutions, BittWare is your partner for everything from a simple accessory board to complete custom variations with complex mechanical requirements. Our resources include the global Molex group to handle any size project.
The ACE software from Achronix is the development environment for the Speedster7t. ACE handles the hardware design workflow, supporting RTL (VHDL and Verilog) input together with industry-standard simulation. ACE also enables using advanced chip features such as the NoC. ACE includes an Achronix-optimized version of Synplify Pro from Synopsys.

Get your S7t card in a TeraBox™ server!
Let us handle the server integration and start your application proof-of-concept without having to dedicate additional valuable resources for setup!

BittWare’s BittWorks II Toolkit:
Powerful Tools for Development
The BittWorks II Toolkit provides drivers, libraries, utilities and example projects for accessing, integrating and developing applications for the S7t.

For more pricing or more information, visit BittWare.com/S7t-VG6

S7t-VG6 Card Specifications

FPGA
- Achronix Speedster AC7t1500
  - 52.5 x 52.5 package
  - 692K 6-input lookup tables (LUTs)
  - 189 Mb embedded RAM
  - 2,560 MLPs

On-board memory
- 8x GDDR6: 8 Gbit per, 2 independent 16 bit channels per; 8 GBytes total
- One bank DDR4-2666 with ECC, 4 GBytes (x72)
- Flash memory for booting FPGA

Host interface
- PCIe Gen3 x16 interface direct to FPGA

External clocking
- 1 PPS and 10MHz ref clk front panel inputs

USB Micro
- USB access to BMC, USB-JTAG, USB-UART

OCuLink
- OCuLink on rear edge, connected to FPGA via 4x transceivers
- PCIe Gen4 Hard IP

GPIO
- 8 GPIO pins, 3.3V, single ended, direction (Tx, Rx) independently settable by FPGA per GPIO, buffers rated to 200Mbps

QSFP cages
- QSFP-DD cage on front panel
  - 56G PAM4 transceivers
  - 1x 400GbE, 2x 200GbE, 4x 100GbE or 8x 10/25/40/50GbE
  - Hard MAC and FEC
- QSFP56 cage on front panel
  - 56G PAM4 transceivers
  - 1x 200GbE, 2x 100GbE or 4x 10/25/40/50GbE
  - Hard MAC and FEC

Board management controller
- Voltage, current, temperature monitoring
- Power sequencing and reset
- Field upgrades
- FPGA configuration and control
- Clock configuration
- I2C bus access
- USB 2.0
- Voltage overrides

Cooling
- Standard: dual-width passive heatsink
- Optional: dual-width active heatsink
- Optional: dual-width liquid cooling

Electrical
- On-board power from two AUX connectors (8 pin)
- Power dissipation is application dependent
- Typical max power consumption TBD

Environmental
- Operating temperature 5°C to 35°C

Form factor
- Standard-height PCIe dual-width board

Development Tools

System development
- Software development toolkit including PCIe driver, libraries, and board monitoring utilities

FPGA development
- Achronix tools—ACE Design Tools
- FPGA example projects

For more pricing or more information, visit BittWare.com/S7t-VG6

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