Achronix

Speedster7t FPGAs

A New Class of FPGAs

Product Highlights

A New Class of FPGA Optimized for High-Bandwidth Workloads

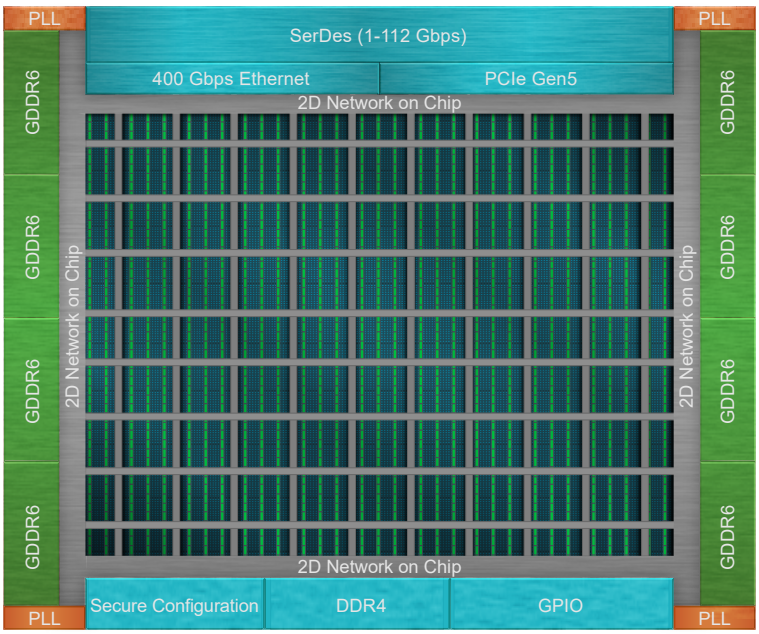
- 326K to 692K 6-input LUTs
- High-performance memory and I/O with up to:
  - 190 Mb of embedded memory
  - 16 channels of GDDR6 with 4 Tbps of high-speed memory bandwidth
  - 32 SerDes lanes supporting data rates of 1 Gbps to 112 Gbps
  - 2 ports of 400G Ethernet (2x 400G or 16x 100G)
  - 2 ports of PCIe Gen5 with x16 and x8
- Revolutionary new two-dimensional network-on-chip (2D NoC) routing structure
- New flexible machine learning processor (MLP) optimized for AI/ML functionality:
  - Delivers up to 61 Int8 TOps
  - Supports multiple floating point and integer numerical format

An Innovative High-Performance FPGA Family

The Achronix Speedster®7t family is built on a revolutionary FPGA architecture that is highly optimized to meet the growing demands of AI/ML, and network intensive and data acceleration applications. The Speedster7t FPGA family features a revolutionary new two-dimensional network-on-chip (2D NoC) and a high-density array of AI/ML-optimized MLPs. Blending FPGA programmability with ASIC-like routing structures and compute engines, the Speedster7t family raises the bar for high-performance FPGAs.

Two-Dimensional Network on Chip Delivers ASIC-Like Performance

Speedster7t FPGAs feature a revolutionary 2D NoC which transports data throughout the FPGA fabric and to high-performance I/O and memory subsystems delivering up to 20 Tbps of aggregate bandwidth. With the 2D NoC, none of the Speedster7t FPGA's programmable-logic is consumed for data transport.



20 Tbps
2D NoC bandwidth

2,560
machine language processors

4 Tbps
high-speed memory bandwidth

692k
6-input LUTs

High-Speed Interfaces

Whether it is to support incoming and outgoing data streams, or storing/buffering that data, high-performance compute, machine learning and hardware acceleration solutions must be able to move data on and off chip. Speedster7t FPGAs have been architected to deliver unprecedented bandwidth.

400G Ethernet

Speedster7t FPGAs support up to 2 ports of 400GbE or 16 ports of 100GbE, connected to the compute fabric via the 2D NoC.

PCI Express Gen5

Speedster7t FPGAs come equipped with multiple PCIe Gen5 interfaces supporting up to 32 Giga transactions per second.

GDDR6

Speedster7t devices are the only FPGAs with embedded support for GDDR6 memories, providing the fastest SDRAM access speeds with the lowest DRAM cost (per stored bit) available. With up to 4 Tbps of GDDR6 bandwidth Speedster7t FPGAs provides memory bandwidth equivalent to an HBM-based FPGA at a fraction of the cost.

DDR4/5

Speedster7t FPGAs include DDR4/5 memory interface support for deeper buffering requirements. The PHY and controller support all standard features defined by the JEDEC specification.

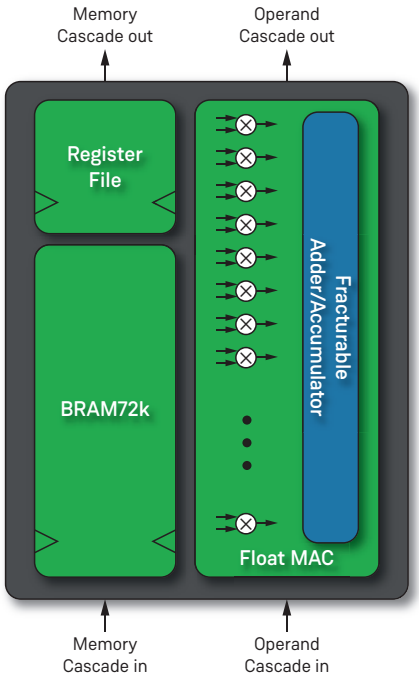
Part Number/Name	AC7t800	AC7t1500
6-input LUTs	326k	692k
Logic elements/system logic cell equivalent	711k LE / 730k LC	1,508k LE / 1,546k LC
Inline cryptography	Yes	–
MLPs (multi-fracturable MAC arrays)	864	2,560
LRAM (2.3 kb)	864	2,560
BRAM (73.7 kb)	1,152	2,560
Memory	85 Mb	190 Mb
ML TOps: int8 or block bfloat16	20.5	61
SerDes	24	32
DDR4/5†	1 DDR5 ×64	1 DDR4 ×64
High-bandwidth memory channels	6 GDDR6†/15 Tbps	16 GDDR6/4 Tbps
PCI Express Gen5	One ×16	One ×8, one ×16
Ethernet	8 lanes 2 × 400G or 8 × 100G	16 lanes 2 × 400G or 16 × 100G
2D NoC bandwidth (Tbps)	12	20

† With ECC.

Machine Learning Processor

Speedster7t FPGAs features programmable math compute elements which are organized into new machine learning processor (MLP) blocks. MLPs are highly configurable, compute-intensive blocks, with up to 32 multiplier/accumulators (MACs), that support 4- to 24 bits integer formats and various floating-point modes including Tensorflow's Bfloat16 format as well as the highly efficient block floating-point format which dramatically increases performance.

MLP blocks include tightly integrated embedded memory blocks to ensure that machine learning algorithms will run at the maximum performance of 750 MHz. This combination of high-density compute and high-performance data delivery results in a processor fabric that delivers the highest usable FPGA-based tera-operations per second (TOps).



Design Tool Support

The Achronix Tool Suite is a tool chain that supports all Achronix hardware products. It works in conjunction with industry-standard synthesis and simulation tools, allowing FPGA designers to easily map their designs into a Speedster7t FPGA.

The Achronix Tool Suite includes an Achronix-optimized version of Synplify Pro from Synopsys and the Achronix Snapshot debugger. Achronix simulation libraries are supported by ModelSim from Siemens EDA, VCS from Synopsys and Riviera-PRO from Aldec.

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