Achronix
Data Acceleration

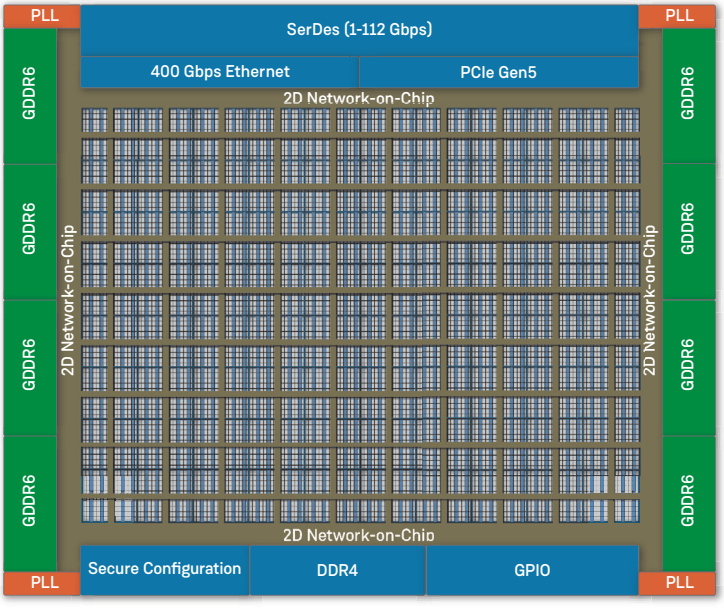
Product Brief

Speedster7t FPGAs

Speedster7t FPGA Highlights

A New Class of FPGA Optimized for High-Bandwidth Workloads

- Built on TSMC 7nm process technology
- 326K to 692K 6-input LUTs
- Up to 190 megabits of embedded memory
- Up to 16 GDDR6 channels delivering up to 4 Tbps of high-speed memory bandwidth
- Up to 32 SerDes lanes supporting data rates up to 112 Gbps
- Up to 4 ports of 400G Ethernet (4× 400G or 16× 100G)
- Up to 2 ports of PCIe Gen5 supporting 16-lane (×16) and 8-lane (×8) configurations
- Revolutionary new two-dimensional network-on-chip (2D NoC) routing structure. With ≥20 Tbps, this functionality fundamentally changes FPGA design methodologies
- New flexible machine learning processor (MLP) optimized for AI/ML functionality:
  - Delivers up to 61 TOps
  - Supports multiple floating point and integer numerical formats



An Innovative High-Performance FPGA Family

The Achronix Speedster®7t family is built on a revolutionary FPGA architecture highly optimized to meet the growing demands of AI/ML and high-bandwidth, data acceleration applications. Specifically designed for these high-bandwidth workloads, the Speedster7t FPGA family features a revolutionary new 2D NoC and a high-density array of AI/ML-optimized MLPs. Blending FPGA programmability with ASIC-like routing structures and compute engines, the Speedster7t family raises the bar on high-performance FPGAs to new levels.

High-Speed Interfaces Support World-Class Bandwidth

Critical for high-performance compute, machine learning and hardware acceleration solutions must be able to move data on and off chip, whether it is to support incoming and outgoing data streams, or storing/buffering that data. Speedster7t FPGAs have been architected to support unprecedented bandwidth.

112 Gbps SerDes

Speedster7t devices have up to 32 of the industry's highest performing SerDes interfaces that can operate up to 112 Gbps.

PCI Express Gen5

Speedster7t FPGAs come equipped with multiple PCIe Gen5 interfaces supporting both 16-lane (×16) and 8-lane (×8) configurations. The PCIe controller interfaces can support either an endpoint or a root complex.

400G Ethernet

Each Speedster7t FPGA includes multiple Ethernet subsystems consisting of eight SerDes lanes and Ethernet MACs to support a range of applications. Each Ethernet MAC is very flexible and can support multiple ports up to 400G, with each SerDes lane able to achieve a line rate between 10 Gbps and 100 Gbps. The high-performance Ethernet interfaces connect to the FPGA fabric through the 2D NoC.

GDDR6

Speedster7t devices are the only FPGAs with embedded support for GDDR6 memories — very high bandwidth at a reasonable cost. Having multiple GDDR6 SDRAM controller ports, Speedster7t FPGAs provide the fastest SDRAM access speeds with the lowest DRAM cost (per stored bit) available.

Each of the GDDR6 memory controllers are capable of supporting 512 Gbps of bandwidth. As a result, with up to 8 GDDR6 controllers in a Speedster7t device, an aggregate GDDR6 bandwidth of 4 Tbps can be supported, delivering the equivalent memory bandwidth of an HBM-based FPGA at a fraction of the cost.

DDR5

Speedster7t FPGAs include DDR5 memory interface support for deeper buffering requirements. The PHY and controller support multiple configurations such as soldered down components on PCB, UDIMM, SODIMM, RDIMM and LRDIMM modules and bit widths from ×4 to ×72. The PHY and controller support all standard features defined by the JEDEC specification and are inter-operable with memories from all major vendors.

New Two-Dimensional Network on Chip Delivers ASIC-Like Performance

Speedster7t FPGAs feature a revolutionary new two-dimensional network-on-chip (2D NoC), designed to support the industry's highest performance interface protocols. The 2D NoC also enables direct connections between the various high-speed networking and memory interfaces. A host processor can transfer data to any of the GDDR6 or DDR5 memory controllers directly from any of the PCIe Gen5 interfaces by simply configuring the 2D NoC for the task. In this use case, none of the FPGA's programmable-logic is consumed because the 2D NoC manages everything — the programmable interconnect within the FPGA array is not required for this data transfer.

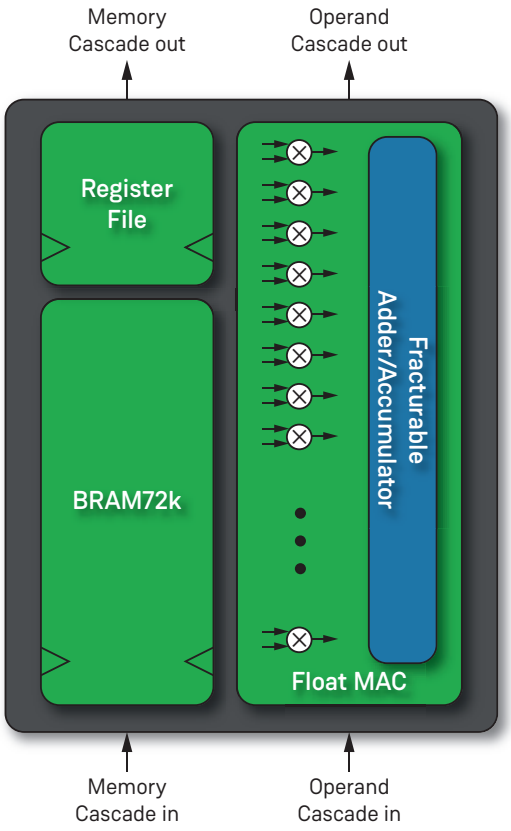
The 2D NoC distributes data throughout the FPGA fabric using a series of high-speed row and column network conduits, distributing data traffic horizontally and vertically throughout the FPGA fabric. Each row or column in the 2D NoC has two 256-bit, unidirectional, industry-standard AXI channels operating at a transfer rate of 512 Gbps in each direction.

Highly Optimized Compute Performance

Each Speedster7t device features a large array of programmable math compute elements which are organized into new machine learning processor (MLP) blocks. Each MLP is a highly configurable, compute-intensive block, with up to 32 multiplier/accumulators (MACs), that support integer formats from 4- to 24-bits and various floating-point modes including native support for Tensorflow's Bfloat16 format as well as the highly efficient block floating-point format which dramatically increases performance.

MLP blocks include tightly integrated embedded memory blocks to ensure that machine learning algorithms will run at the maximum performance of 750 MHz. This combination of high-density compute and high-performance data delivery results in a processor fabric that delivers the highest usable FPGA-based tera-operations per second (TOps).

Speedster7t Machine Learning Processor



Security Comes Built In

To confront the threat of third-party attacks, Speedster7t FPGAs come equipped with the most advanced bitstream security features with multiple layers of defense for protecting bitstream secrecy and integrity. Keys are encrypted based on a tamper-resistant, physically unclonable function (PUF), and bitstreams are encrypted and authenticated using 256-bit AES-GCM. To defend against side-channel attacks, bitstreams are segmented, with separately derived keys used for each segment. The decryption hardware employs differential power analysis (DPA) counter measures. Additionally, a 2048-bit RSA public key authentication protocol is used to activate the decryption and authentication hardware. Users can be confident that when they load their secure bitstream, it is the intended configuration because it has been authenticated by RSA public key, AES-GCM private key, and a CRC checksum.

Design Tool Support

The Achronix Tool Suite is a state-of-the-art tool chain that supports all Achronix hardware products. ACE works in conjunction with industry-standard synthesis and simulation tools, allowing FPGA designers to easily map their designs into Speedster7t FPGAs, and Speedcore eFPGAs.

In addition to ACE, the Achronix Tool Suite includes an Achronix-optimized version of Synplify-Pro from Synopsys and the Achronix Snapshot debugger. Achronix simulation libraries are supported by ModelSim from Siemens EDA, VCS from Synopsys and Riviera-PRO from Aldec.

Proven Conversion Path to Low-Cost ASIC for High-Volume Requirements

Achronix is the only company that offers both standalone FPGAs and embedded FPGA (eFPGA) IP. The Speedcore™ eFPGA IP is the same technology that Achronix uses in its Speedster7t FPGAs, enabling a seamless conversion from Speedster7t FPGA to an ASIC design. FPGA applications typically have functions that must remain programmable while other functional blocks can be fixed function. For ASIC conversions, those fixed functions can be hardened into the ASIC structure, reducing die size, cost and power. Customers can expect to get up to a 50 percent power reduction and 90 percent cost reduction when they use Speedcore eFPGA IP to convert Speedster7t FPGAs to an ASIC.

About Achronix Semiconductor Corporation

Achronix Semiconductor Corporation is a fabless semiconductor corporation based in Santa Clara, California, offering high-end FPGA-based data acceleration solutions, designed to address high-performance, compute-intensive and real-time processing applications. Achronix is the only supplier to have both high-performance, high-density standalone FPGAs and licensed eFPGA IP solutions. Achronix Speedster®7t FPGA and Speedcore™ eFPGA IP offerings are further enhanced by ready-to-use VectorPath™ accelerator cards targeting AI, machine learning, networking and data center applications. All Achronix products are fully supported by the Achronix Tool Suite which enables customers to quickly develop their own custom applications.

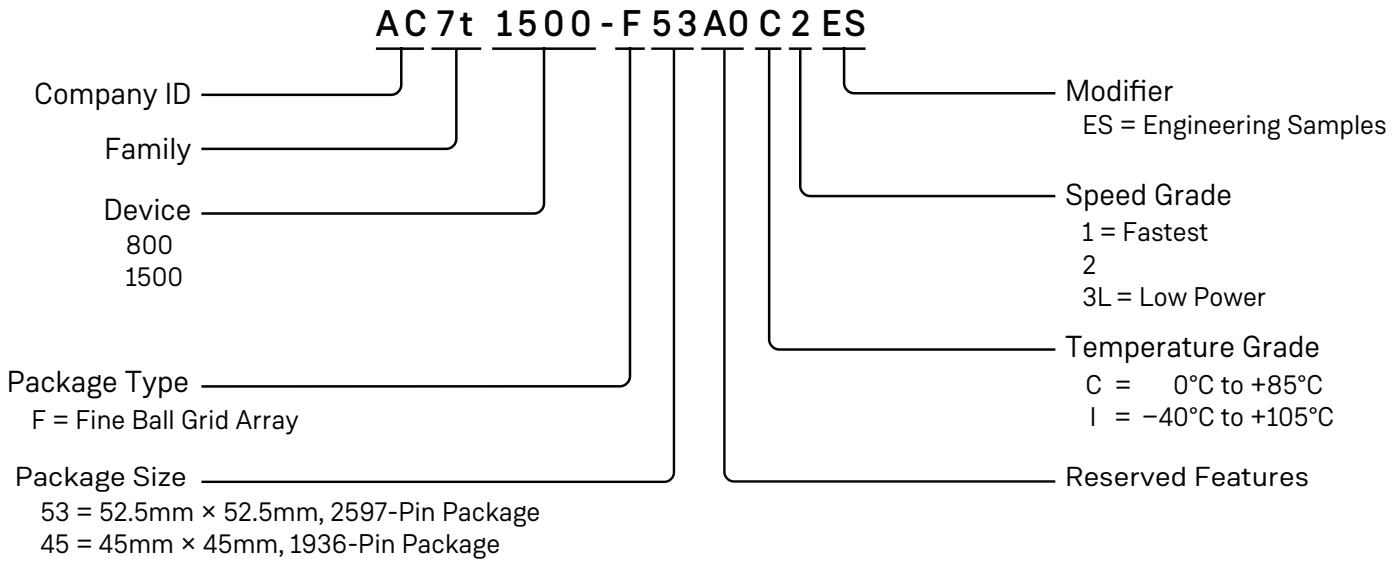
Achronix has a global footprint, with sales and design teams across the U.S., Europe and Asia. For more information, please visit www.achronix.com.

Speedster7t Family Table

Part Number/Name	AC7t800	AC7t1500
6-input LUTs	326k	692k
Inline cryptography	Yes	–
MLPs (multi-fracturable MAC arrays)	864	2,560
LRAM (2 kb)	288	2,560
BRAM (72 kb)	1,152	2,560
Memory	85 Mb	190 Mb
ML TOps: int8 or block bfloat16	20.5	61
SerDes 112G	24	32
DDR4/5(†)	1 DDR5 ×64	1 DDR4 ×64
High-bandwidth memory channels	6 GDDR6(†)/15 Tbps	16 GDDR6/4 Tbps
PCI Express Gen5	One ×16	One ×8, one ×16
Ethernet	8 lanes 2 × 400G or 8 × 100G	16 lanes 4 × 400G or 16 × 100G
2D NoC bandwidth (Tbps)	12	20

† With ECC.

Speedster7t Ordering Codes



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