Speedster7t Power User Guide

For Speedster7t Devices

Achronix®

Data Acceleration

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Chapter - 1: Introduction

This document describes the different power supplies that are required for the Speedster7t 7t1500 device and voltage tolerance levels for each of them. Also included are the connection guidelines for each of the power rails and recommendations for the power supply network sharing schemes at the board level.

Chapter - 2: Power Supply Requirements

The table below provide a list of power supplies used in Speedster7t devices, connection guidelines and tolerance levels for each of these supplies.

Table 1: ***Speedster7t Power Supplies***

Pin Name	Description	Connection Guidelines	Minimum Voltage (V)	Typical Voltage (V)	Maximum Voltage (V)	AC Ripple (mV)
CLKIO_[NE/NW/SE/SW]_VDDIO	Analog supply for clock I/O	The CLKIO power supply can be set to either of these supplies, 1.8V or 1.5V. The I/O standard can be configured at clock bank corner granularity (NW/NE/SW /SE).(1)	1.485	1.5	1.515	±15 mV
			1.782	1.8	1.818	±18 mV
CLKIO_[NE/NW/SE/SW]_VREF	Reference voltage supply for the CLKIO	The reference voltage for the CLKIO can either be generated using a macro or can be driven by an external supply. If using an external supply, connect this pin to CLKIO_*_VDDIO/2	0.7425	0.75	0.7575	±7.5 mV
			0.891	0.9	0.909	±9 mV
CORE_VDD	Power supply for the FPGA fabric	Power supply for the fabric based on the selected speed grade. • C1 – 0.90V • C2 – 0.85V • C3L – 0.75V	0.891	0.90	0.909	±9 mV
			0.841	0.85	0.859	±8.5 mV
			0.74	0.75	0.759	±7.5 mV
DDR4_S0_VAA	Analog supply for the DDR PLL	Connect to a 1.8V linear or low-noise switching power supply.(2)	1.782	1.8	1.818	±18 mV
DDR4_S0_VDDQ	I/O domain power supply for the DDR4 PHY	Connect to a 1.2V linear or low-noise switching power supply.(2)	1.159	1.2	1.241	±19 mV
ENOC_[N/NE/NW/S/SE/SW]_PLL_VDDA	Analog supply for the NoC PLLs	Dedicated power supply for each PLL. Requires an RC filtered 1.8V power supply from the board.	1.782	1.8	1.818	±18 mV
ENOC_[N/NE/NW/S/SE/SW]_PLL_VSSA	Ground power supply for the NoC PLLs	Common ground supply for the peripheral NoC and GCG PLLs.(3)		0		
FUSE_VDD2	Analog supply for the eFUSE module	Connect to a 1.8V linear or low-noise switching power supply.	1.782	1.8	1.818	±18 mV
FCU_VDDIO	Analog supply for the GPIO associated with FCU/JTAG	Connect to a 1.8V power supply. This supply can be shared with CLKIO_*_VDDIO supply if a 1.8V standard is used for the CLKIO.	1.782	1.8	1.818	±18 mV

Pin Name	Description	Connection Guidelines	Minimum Voltage (V)	Typical Voltage (V)	Maximum Voltage (V)	AC Ripple (mV)
GCG_[NE/NW/SE/SW]_PLL_VDDA	Analog supply for the clock generator PLLs	Dedicated power supply for each PLL. Requires an RC filtered 1.8V power supply from the board.	1.782	1.8	1.818	±18 mV
GCG_[NE/NW/SE/SW]_PLL_VSSA	Ground power supply for the Clock Generator PLLs	Common ground supply for the peripheral NoC and GCG PLLs.(3)		0		
GDDR6_[E/W]_VDDR	Digital supply for GDDR6 PHY. This supply is used for level shifting input signals from VDDR to VDDA domain and all output signals from VDDA to VDDR domain.	Connect to a 0.85V supply. The GDDR6_VDDA supply can be shared with GDDR6_VDDR with a filter in between.	0.825	0.85	0.875	±17 mV
GDDR6_[E/W]_VDDA	Analog power supply for GDDR6 PHY. This supply is used for digital logic, custom digital, data pipes and receive delay lines. Also used as analog circuit supply, clocking, global and local clock trees.		0.833	0.85	0.867	±8.5 mV
GDDR6_[E/W]_VDDIO	GDDR6 I/O power supply	Connect to a 1.35V supply. The GDDR6_VDDIO supply can be shared with GDDR6_VDDP with a filter in between.	1.32	1.35	1.377	±13.5 mV
GDDR6_[E/W]_VDDP	PLL supply for GDDR6 PHY		1.32	1.35	1.377	±13.5 mV
GPIO_[N0/S0]_VDDIO	Analog supply for the GPIO	The GPIO power supply can be set to one of these supplies: 1.8V, 1.5V, 1.35V, 1.2V, or 1.1V. The I/O standard can be configured at corner granularity (NW/NE/SW/SE).(1)	1.089	1.1	1.11	±11 mV
			1.188	1.2	1.212	±12 mV
			1.336	1.35	1.363	±13.5 mV
			1.485	1.5	1.515	±15 mV
			1.782	1.8	1.818	±18 mV
GPIO_[N0/S0]_VREF	Reference voltage supply for the GPIO	The reference voltage for the GPIO can either be generated using a macro or can be driven by an external supply. If using an external supply, connect this pin to GP IO_*_VDDIO/2	0.545	0.55	0.556	±5.5 mV
			0.594	0.6	0.606	±6 mV
			0.668	0.675	0.682	±6.7 mV
			0.742	0.75	0.757	±7.5 mV
			0.891	0.9	0.909	±9 mV
SRDS_N_PA_VDDH	SerDes analog high-power supply	1.2V analog power supply for the SerDes.(4)	1.19	1.2	1.2096	±4.8 mV

Pin Name	Description	Connection Guidelines	Minimum Voltage (V)	Typical Voltage (V)	Maximum Voltage (V)	AC Ripple (mV)
SRDS_N_PA_VDDL	SerDes analog low-power supply	0.75V Analog power supply for the SerDes.(4)	0.74	0.75	0.759	±4.9 mV
SRDS_N_PA_VSS	SerDes ground	Ground power supply for the SerDes lanes.		0		
TS_VDDA	Analog power supply to the temperature sensor	Connect to a 1.8V power supply. This supply can be shared with PLL_VDDA or FUSE_VDD2 power supply.	1.782	1.8	1.818	±18 mV
VCC	Digital supply for the GDDR6 controller, DDR4 PHY and controller, Achronix PCS and the eFuse module	0.75V digital power supply.	0.74	0.75	0.76	±7.5 mV
VSS	Ground	All GND pins should be connected to the board's ground plane.		0		

Table Notes

1. Unused I/O banks should be powered — power balls should not be left floating or grounded.
2. The maximum supply ramp rate should be limited to 5 mV/µs.
3. PLL VSSA should not be shorted with any other VSS supply.
4. Connect these pins to a linear or low-noise switching power supply.

Chapter - 3: Power Supply Block Diagram

The diagram below represents power sharing scheme for a use-case scenario that helps to reduce the required number of power supplies. The number can be further reduced depending upon the targeted speed grade of the device (see notes below). The sharing schemes are subject to change based on the user's design requirements.

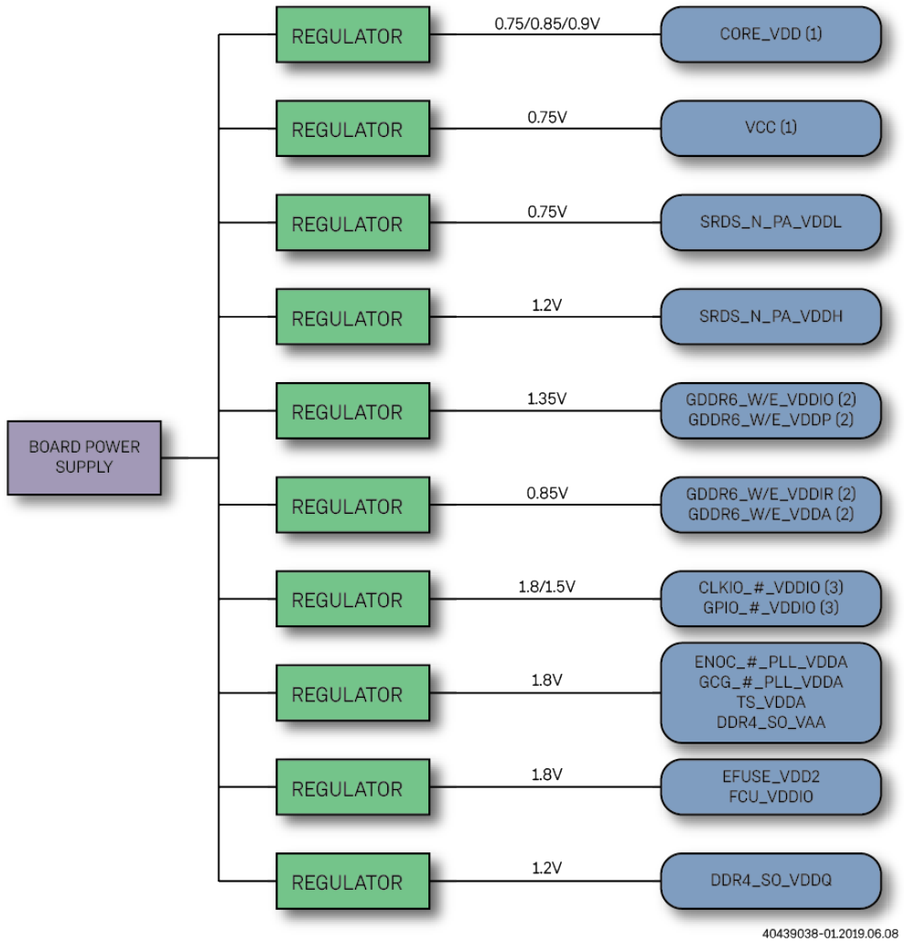

Figure 1: ***Speedser7t Power Supplies***

Figure Notes

1. The CORE_VDD and VCC supplies can be shared on the C3L speed-grade devices where the nominal voltages for these two rails are the same.
2. The GDDR6_W/E_VDDIO and GDDR6_W/E_VDDP supplies can be shared with a filter in between them. Similarly, GDDR6_W/E_VDDR and GDDR6_W/E_VDDA supplies can be shared with a filter in between them.
3. CLK_#_VDDIO and the GPIO_#_VDDIO can be shared, provided both I/O groups are configured to use 1.8V or 1.5V. If different power supplies are desired for each of the I/O groups, these supplies cannot be shared.

Chapter - 4: Power Sequencing

There is only a single power sequencing requirement applicable for the Speedster7t family of devices. The VCC power supply should be brought up before the EFUSE_VDD2 (1.8V) and pulled down after EFUSE2_VDD2 is pulled down. This sequencing is to ensure that there is no unwanted leakage when powering up the device.

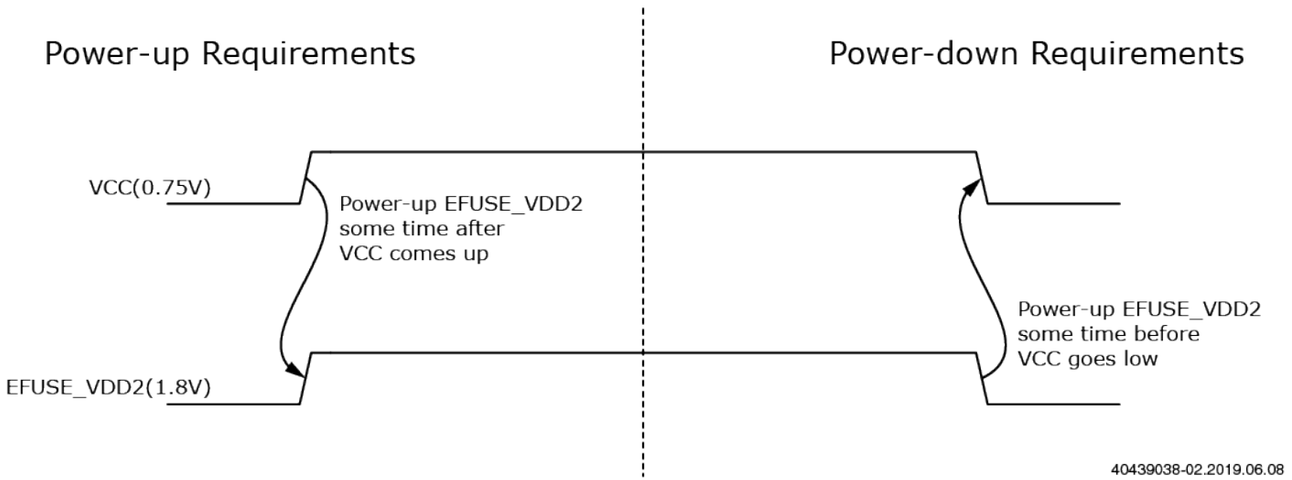

Figure 2: ***Speedster7t Power Sequencing***

Chapter - 5: Revision History

Version	Date	Description
1.0	27 Jun 2019	• Initial Achronix release.