Speedster7t Power Estimator User Guide (UG093)

Speedster FPGAs

Preliminary Data

Achronix®
Data Acceleration

Copyrights, Trademarks and Disclaimers

Preliminary Data

This document contains preliminary information and is subject to change without notice. Information provided herein is based on internal engineering specifications and/or initial characterization data.

Achronix Semiconductor Corporation

2903 Bunker Hill Lane
Santa Clara, CA 95054
USA

Website: www.achronix.com
E-mail : info@achronix.com

Table of Contents

Chapter - 1: Introduction

The Achronix Speedster®7t Power Estimator tool provides a platform to calculate the power requirements for the Achronix 7nm standalone FPGAs. This user guide gives a detailed overview of the thermal and power needs depending on the device, environment and utilization of components in the design. The power estimator tool can be used at any stage of the design process to obtain an estimate of the total power dissipation from the device. However, it is generally used early on, prior to actual design activity, to obtain a first-cut estimate of the power needs so that board regulators and thermal solutions can be designed accordingly and power integrity analyses done appropriately. This estimate could then be compared with post-implementation results using the ACE-generated power report.

The Achronix Speedster Power Estimator is a spreadsheet that takes parameters as user inputs to estimate the total power dissipated. This includes device characteristics, thermal characteristics and utilization of IP resources such as BRAMs, LRAMs, MLPs, LUTs, etc. To obtain a good estimate of the design's power profile, the user is required to enter a realistic estimate of the design utilization.

Since this estimator is used at a very early stage of the design process, it is probable that the user cannot yet account for all the worst-case scenarios while providing inputs to the tool, for example, junction temperature for static power measurement and toggle rate inputs for different modules. Even slight temperature variations, especially in the higher order, could result in significant changes in the static power while providing toggle rates not accounting for realistic worst cases could result in underestimating dynamic power. In order to cover for such cases, it is recommended that the user adds an additional guard band of 30% to the total power estimation when specifying power regulators for the board.

Chapter - 2: System Requirements and Setup

The Achronix Speedcore Power Estimator tool is compatible with Microsoft Excel 2007 and later versions. By default, the spreadsheet's security setting disables macros when opened. These macros must be enabled in order to use this spreadsheet. This setting can be changed when opening the spreadsheet.

For Excel versions 2007 and 2010:

1. Opening the spreadsheet first displays a security warning banner. Click **Options...** to proceed.
2. From the Microsoft Office Security Options popup window displaying "Security Alert - Macro," select **Enable this content** followed by clicking **OK** to close the window.

For Excel versions 2013 and 2016:

1. Opening the spreadsheet first displays a protected view warning banner. Click **Enable Editing** to proceed.
2. Then a security warning banner displaying "Macros have been disabled." Click **Enable Content** to proceed.

Chapter - 3: Speedster7t Power Estimator UG Power Central Worksheet

The central power estimator worksheet is the main worksheet of the estimator where the breakdown of various power dissipation components is displayed. It is divided into four sections: System Variables, Power Usage by Resource, Current by Power Supply and Power Usage Summary.

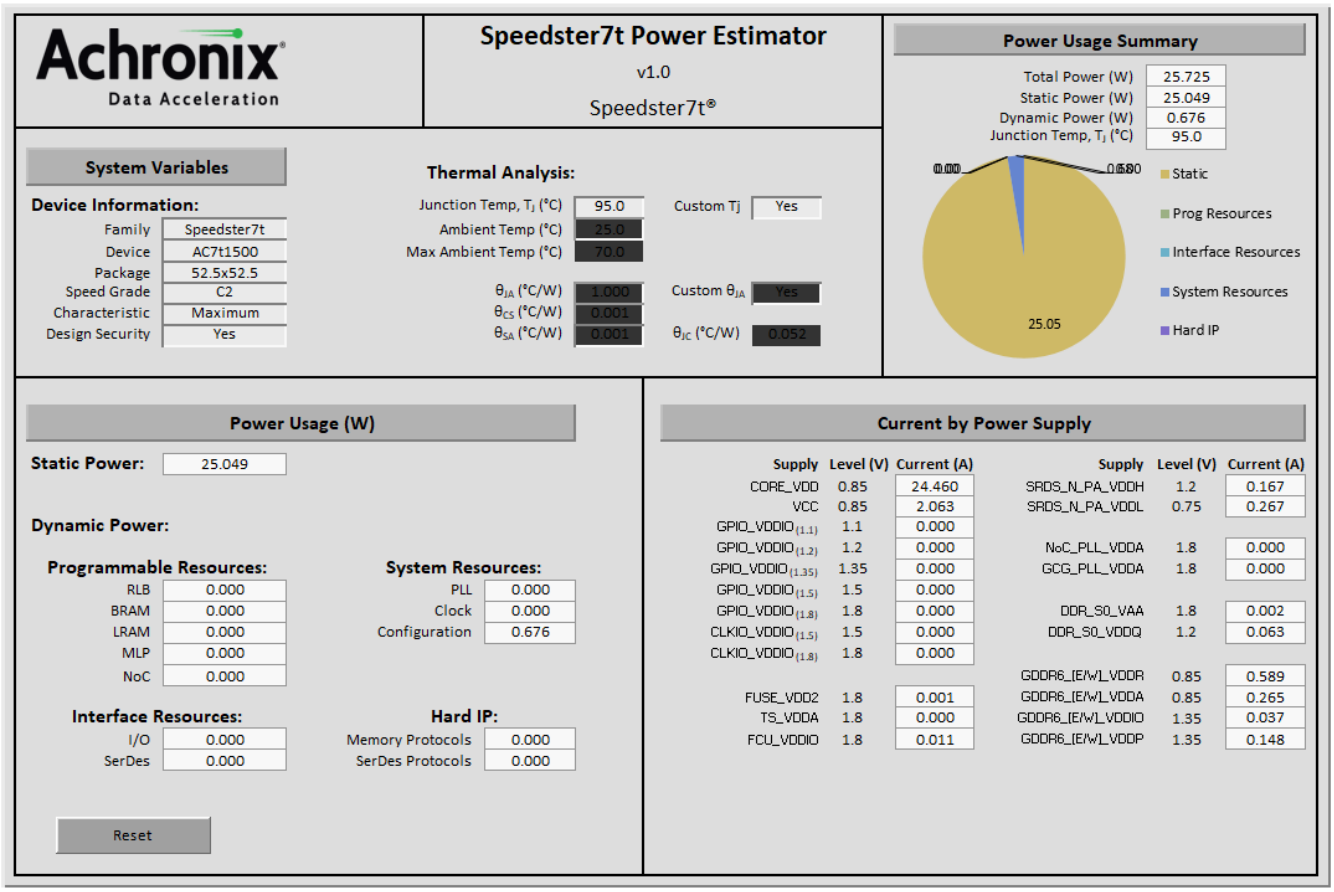


Figure 1: *Power Central Worksheet*

System Variables

This section includes two parts: Device Information and Thermal Analysis.

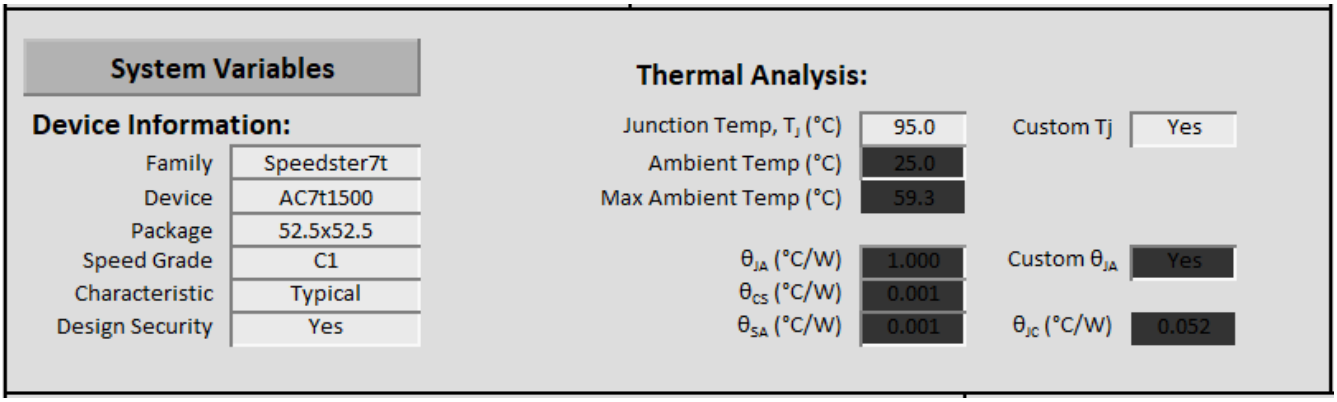


Figure 2: ***System Variables Section***

Device Information

The Device Information section allows the user to provide top-level device characteristics to be used in power calculations in the rest of the spreadsheet. It takes in the following input parameters to calculate power.

Table 1: ***System Variables Input Parameters***

Parameter	Description
Family	Achronix Speedster7t device family.
Device	Speedster7t device variant in the family.
Package	Package dimensions of the chosen device
Speed Grade	This option allows the user to select the desired speed grade for the target device: C1/C2/C3. The operating voltage corresponding to these speed grades are as below: • C1 – 0.9V • C2 – 0.85V • C3 – 0.75V **Note** C1 offers the fastest speed grade for the selected device under normal conditions
Characteristic	This option allows the user to select the device characteristics used for static power calculation: • Typical – power dissipation characteristics of a device considered to be the median in the device power distribution. • Maximum – power dissipation characteristics of the worst-case device in the power distribution. In order to account for worst-case process variation, it is recommended to set the characteristics to Maximum.

Parameter	Description
Design Security	This option allows the user to enable or disable design security feature, i.e, if the application requires fuse blowing (e,g., programming encryption fuses for design security).

Thermal Analysis

This section allows for device thermal characteristics to be calculated to:

- Ensure that device maximum junction temperature specifications are not exceeded.
- Appropriate thermal solutions (heat sinks and fans) can be devised.
- Provide an output junction temperature that allows for static and total power calculations to help drive board regulator solutions.

The following input parameters can be modified based upon the end requirements.

Table 2: *Thermal Analysis Input Parameters*

Parameter	Description
Junction Temperature, T_J (^oC)	The junction or operating temperature refers to the temperature of the silicon die within the package of the device when the device is powered. $T_J = T_A + (P \times \Theta_{JA})$ where T_J is the Junction temperature in ^oC, T_A is the ambient temperature in ^oC, P is the total power dissipated in Watts and Θ_{JA} is the junction-to-ambient thermal resistance in $^oC/W$.
Custom T_J	Allows the user to enable/disable user-defined T_J. When custom T_J is disabled, the junction temperature is calculated based on the formula above and when enabled, the user has the choice to enter a predetermined value.
Ambient temperature, (^oC)	The ambient temperature refers to the temperature of the surrounding environment (typically air) when the device is powered. This field can only be accepted as an input if the custom T_J option is disabled or set to 'No'.
Max Ambient temperature, (^oC)	The maximum ambient temperature should be such that the junction temperature does not exceed the maximum allowed for the device. Refer to the datasheet for the temperature range supported by the target Speedster7t device.
Custom Θ_{JA}	When this option is enabled, it allows the user to enter a predetermined value for Θ_{JA} keeping the other thermal resistance values unchanged. When disabled, the user is required to enter values for Θ_{JC}, Θ_{CS} and Θ_{SA} to have Θ_{JA} be calculated automatically.
Θ_{JA} (°C/W)	Junction-to-ambient thermal resistance. The user has the option to provide a custom value for this value or have it be calculated with the formula $\Theta_{JA} = \Theta_{JC} + \Theta_{CS} + \Theta_{SA}$ based on the option chosen for 'Custom Θ_{JA}'.

Parameter	Description
Θ_{JC} (°C/W)	Junction-to-case thermal resistance. Only used when 'Custom Θ_{JA}' is disabled or set to 'No'.
Θ_{CS} (°C/W)	Case-to-heat sink thermal resistance. Only used when 'Custom Θ_{JA}' is disabled or set to 'No'.
Θ_{SA} (°C/W)	Heat sink-to-ambient thermal resistance. Only used when 'Custom Θ_{JA}' is disabled or set to 'No'.

Power Usage

The Power Usage section presents the total power breakdown in terms of Static Power and Dynamic Power based on the resources.

Static Power

Static power or standby power is the power dissipated when the device is in an unconfigured state after power-up. It depends on the device selected (die area), process characteristics, temperature and operating voltages.

Dynamic Power

The dynamic or switching power dissipation is caused by switching activity inside the Speedster7t FPGA and is a function of switching frequency, operating voltage and load. This section gives a breakdown of the different power dissipation sources that contribute to the dynamic power in the device:

Programmable Resources

This section summarizes the power dissipated by the total RLBs, BRAMs, LRAMs, NOC and MLP components in the device. Each of these components has a separate worksheet for power calculation which will be explained in detail later in this document

Interface Resources

This section includes power dissipated by I/O and SerDes interfaces in the device. Each of these components has a separate worksheet for power calculation which will be explained in detail later in this document.

System Resources

This includes power dissipated by the total PLLs and clocks used in the design and also the configuration power. The configuration power is the total power consumed from initial power-up to user mode.

Hard IP

This section lists the power consumed by the hard IP used in the design. They are split into the following protocols accordingly.

Memory Protocols

This section includes the power consumed by the DDR and the GDDR6 controller subsystems.

SerDes Protocols

This section includes the power consumed by the other SerDes-based hard IP such as Ethernet and PCI Express. A more detailed review of the hard IP are addressed in the Hard IP worksheet later in this document

The Power Usage section also has a '**Reset**' option that enables the user to clear all user-defined inputs and from the spreadsheet and set the toggle rates to the default value.

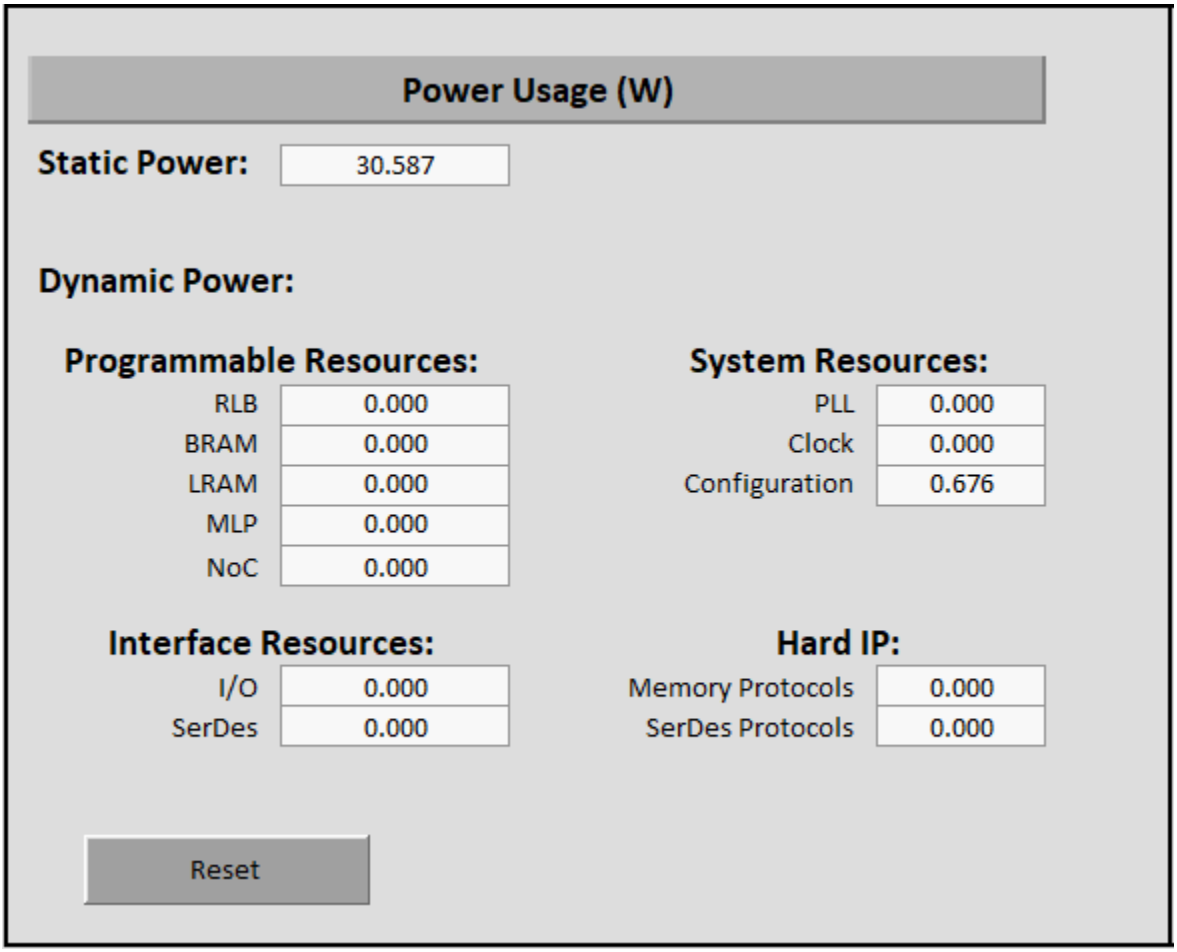


Figure 3: ***Power Usage by Resources***

Current by Power Supply

The Current by Power Supply section provides the user a breakdown of the total current that is the sum of both the static and dynamic current components used by each of the voltage rails present in the device. The voltage level corresponding to the voltage rails are also displayed.

Current by Power Supply

Supply	Level (V)	Current (A)	Supply	Level (V)	Current (A)
CORE_VDD	0.85	34.262	SRDS_N_PA_VDDH	1.2	0.234
VCC	0.85	2.890	SRDS_N_PA_VDDL	0.75	0.374
GPIO_VDDIO (1.1)	1.1	0.000			
GPIO_VDDIO (1.2)	1.2	0.000	NoC_PLL_VDDA	1.8	0.000
GPIO_VDDIO (1.35)	1.35	0.000	GCG_PLL_VDDA	1.8	0.000
GPIO_VDDIO (1.5)	1.5	0.000			
GPIO_VDDIO (1.8)	1.8	0.000	DDR_S0_VAA	1.8	0.002
CLKIO_VDDIO (1.5)	1.5	0.000	DDR_S0_VDDQ	1.2	0.088
CLKIO_VDDIO (1.8)	1.8	0.000			
			GDDR6_[E/W]_VDDR	0.85	0.826
FUSE_VDD2	1.8	0.002	GDDR6_[E/W]_VDDA	0.85	0.372
TS_VDDA	1.8	0.000	GDDR6_[E/W]_VDDIO	1.35	0.052
FCU_VDDIO	1.8	0.015	GDDR6_[E/W]_VDDP	1.35	0.208

Figure 4: ***Current by Power Supply***

Power Usage Summary

This section provides a summary of all the power dissipation components such as the Total Power (W), Static Power (W) and Dynamic Power (W) and their distribution across various device resources on a pie chart. This provides a pictorial representation of the percentage contribution of each of these resources towards the total power dissipated by the device.

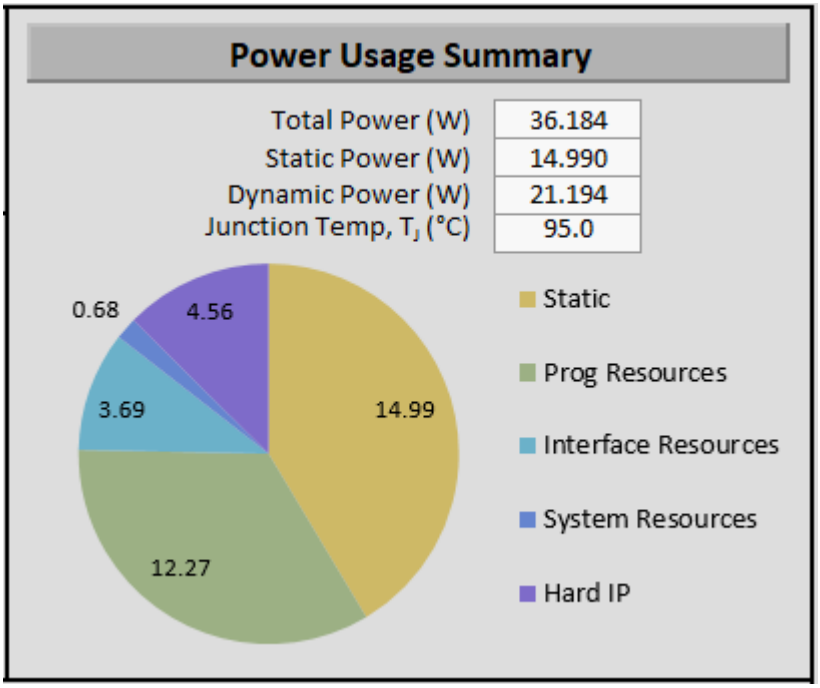
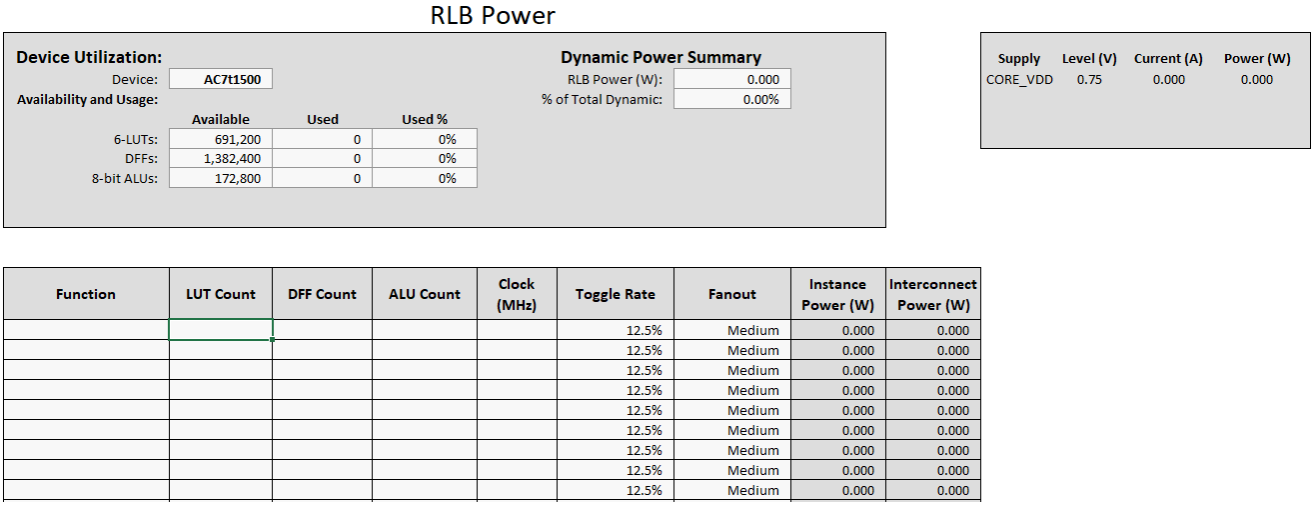


Figure 5: ***Power Usage Summary***

Chapter - 4: Speedster7t Supporting Estimator Worksheets

RLB Worksheet

The RLB power worksheet provides a summary of the total RLB utilization that comprises the LUTs, DFFs and ALUs in the design versus the available resource count in the device. The worksheet also lists the total dynamic power consumed by these RLB logic components in the design. Based on the values entered by the user in the following fields, the worksheet computes the total dynamic power as a sum of the total instance and interconnect power of all the RLB logic used and the corresponding dynamic current for the chosen CORE_VDD rail.



RLB Power

Device Utilization:

Device: AC7t1500

Availability and Usage:

	Available	Used	Used %
6-LUTs:	691,200	0	0%
DFFs:	1,382,400	0	0%
8-bit ALUs:	172,800	0	0%

Dynamic Power Summary

RLB Power (W): 0.000

% of Total Dynamic: 0.00%

Supply	Level (V)	Current (A)	Power (W)
CORE_VDD	0.75	0.000	0.000

Function	LUT Count	DFF Count	ALU Count	Clock (MHz)	Toggle Rate	Fanout	Instance Power (W)	Interconnect Power (W)
					12.5%	Medium	0.000	0.000
					12.5%	Medium	0.000	0.000
					12.5%	Medium	0.000	0.000
					12.5%	Medium	0.000	0.000
					12.5%	Medium	0.000	0.000
					12.5%	Medium	0.000	0.000
					12.5%	Medium	0.000	0.000
					12.5%	Medium	0.000	0.000
					12.5%	Medium	0.000	0.000

Figure 6: *RLB Power Worksheet*

Table 3: *RLB Power Worksheet Fields*

Name	Description
Input Fields	
Function	Description about the functionality/module associated with the LUT. This entry is optional.
LUT Count	The number of LUTs used in the functions/modules of the design.
DFF Count	The total register count used in the functions/modules of the design.
ALU Count	The total number of ALUs used in the functions/modules of the design
Clock (MHz)	The clock frequency associated with the LUTs/registers in that portion of the circuitry.

<table>
<tr><th>Name</th><th>Description</th></tr>
<tr><td>Toggle rate</td><td>The percentage at which the logic or data toggles on each clock cycle. More information on how to estimate toggle rates can be found in the application note Measuring Accurate Toggle Rates (AN010).</td></tr>
<tr><td>Fanout</td><td>The average number of fanout nets driven by the LUTs, ALUs and registers. The values are very low, low, medium, high and very high and the corresponding fanout limits are
<table>
<tr><th>Option</th><th>Fanout</th></tr>
<tr><td>very low</td><td>1 to 2</td></tr>
<tr><td>low</td><td>3 to4</td></tr>
<tr><td>medium</td><td>5 to 8</td></tr>
<tr><td>high</td><td>9 to 12</td></tr>
<tr><td>very high</td><td>greater than 12</td></tr>
</table></td></tr>
<tr><td colspan="2">Calculated Fields</td></tr>
<tr><td>Instance Power (W)</td><td>Calculation of the total power used by the LUTs, ALUs and registers for a particular function /module. These values are then summed to provide the total in the summary section.</td></tr>
<tr><td>Interconnect Power (W)</td><td>Total dynamic power contributed by the interconnect to/from LUTs, ALUs and registers</td></tr>
</table>

BRAM Worksheet

The BRAM worksheet summarizes the total BRAMs used as a percentage of the total available BRAMs. It also shows the sum of instance and interconnect power as the total dynamic power dissipation from BRAM usage based on the user-specified inputs and highlights it as a percentage of the total dynamic power. This worksheet also shows the corresponding total dynamic current for the chosen CORE_VDD rail.

BRAM Power

Device Utilization:

Device:	AC7t1500	
Available BRAMs:	2,560	
Used BRAMs:	0	0%

Dynamic Power Summary

BRAM Power (W):	0.000
% of Total Dynamic:	0.00%

Supply	Level (V)	Current (A)	Power (W)
CORE_VDD	0.75	0.000	0.000

Function	BRAM Count	Mode	Port A			Port B			Instance Power (W)	Interconnect Power (W)
			Data Org	Clock (MHz)	Toggle Rate	Data Org	Clock (MHz)	Toggle Rate		
		Simple Dual Port	x72		25.0%	x72		25.0%	0.000	0.000
		Simple Dual Port	x72		25.0%	x72		25.0%	0.000	0.000
		Simple Dual Port	x72		25.0%	x72		25.0%	0.000	0.000
		Simple Dual Port	x72		25.0%	x72		25.0%	0.000	0.000
		Simple Dual Port	x72		25.0%	x72		25.0%	0.000	0.000
		Simple Dual Port	x72		25.0%	x72		25.0%	0.000	0.000
		Simple Dual Port	x72		25.0%	x72		25.0%	0.000	0.000
		Simple Dual Port	x72		25.0%	x72		25.0%	0.000	0.000
		Simple Dual Port	x72		25.0%	x72		25.0%	0.000	0.000
		Simple Dual Port	x72		25.0%	x72		25.0%	0.000	0.000
		Simple Dual Port	x72		25.0%	x72		25.0%	0.000	0.000
		Simple Dual Port	x72		25.0%	x72		25.0%	0.000	0.000

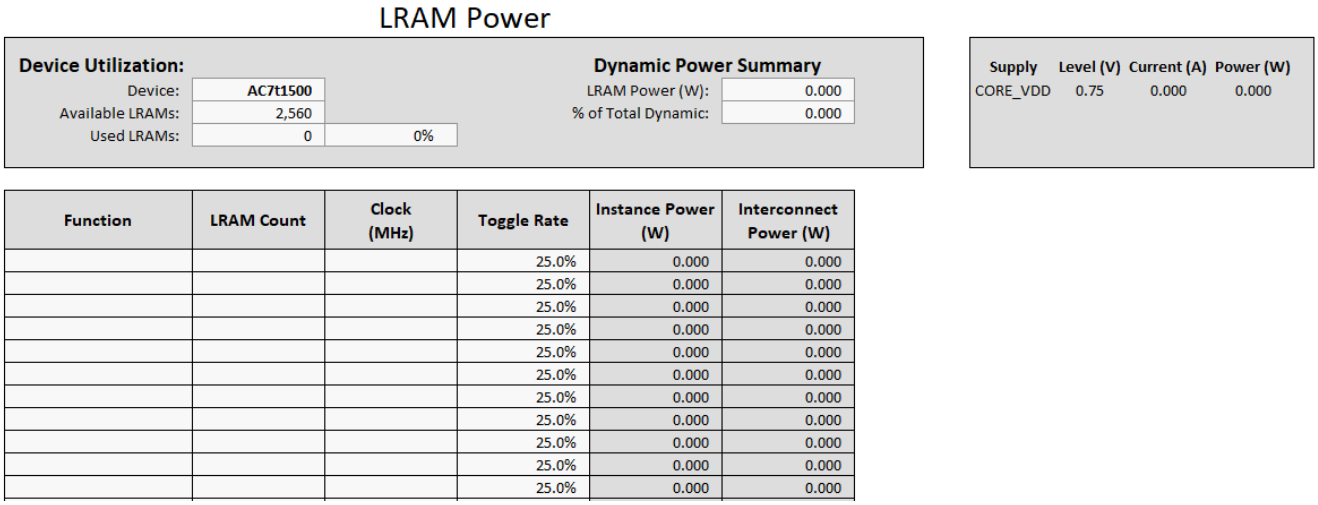
Figure 7: ***BRAM Power Worksheet***

Table 4: *BRAM Power Worksheet Fields*

Name	Description
Input Fields	
Function	Description about the functionality/module associated with the BRAM. This entry is optional.
BRAM Count	The number of BRAMs used in the function/module of the design.
Mode	BRAM mode of operation is one of: ROM, simple dual port or FIFO. A simple dual-port RAM has one read port and one write port, ROMs are read-only RAMs, and FIFOs are the BRAMs used for FIFO implementation.
Data Org	The data width of BRAMs for ports A and B. The values range from ×4 to ×144.
Clock (MHz)	The clock frequencies for the BRAMs at ports A and B in those modules.
Toggle Rate	The percentage at which the BRAM toggles on each clock cycle on ports A and B.
Calculated Fields	
Instance Power (W)	Calculation of the total power used by the BRAMs for a particular function/module.
Interconnect Power (W)	Total dynamic power contributed by the interconnect to/from BRAMs.

LRAM Worksheet

The LRAM worksheet summarizes the total LRAMs used as a percentage of the total available LRAMs. It also shows the sum of instance and interconnect power as the total dynamic power dissipation from LRAM usage based on the user-specified inputs and highlights it as a percentage of the total dynamic power. This worksheet also shows the corresponding total dynamic current for the chosen CORE_VDD rail.



LRAM Power

Device Utilization:			Dynamic Power Summary	
Device:	AC7t1500		LRAM Power (W):	0.000
Available LRAMs:	2,560		% of Total Dynamic:	0.000
Used LRAMs:	0	0%		

Supply	Level (V)	Current (A)	Power (W)
CORE_VDD	0.75	0.000	0.000

Function	LRAM Count	Clock (MHz)	Toggle Rate	Instance Power (W)	Interconnect Power (W)
			25.0%	0.000	0.000
			25.0%	0.000	0.000
			25.0%	0.000	0.000
			25.0%	0.000	0.000
			25.0%	0.000	0.000
			25.0%	0.000	0.000
			25.0%	0.000	0.000
			25.0%	0.000	0.000
			25.0%	0.000	0.000
			25.0%	0.000	0.000
			25.0%	0.000	0.000

Figure 8: ***LRAM Power Worksheet***

Table 5: ***LRAM Power Worksheet Fields***

Input Parameter	Description
Input Fields	
Function	Description about the functionality/module associated with the LRAM. This entry is optional.
LRAM Count	The number of LRAMs used in the function/module of the design.
Clock (MHz)	The clock frequency for the LRAM used in this circuitry.
Toggle Rate	The percentage at which the LRAM data toggles on each clock cycle for that module.
Calculated Fields	
Instance Power (W)	Calculation of the total power used by the LRAMs for a particular function/module.
Interconnect Power (W)	Total dynamic power contributed by the interconnects to/from LRAMs

MLP Worksheet

The MLP worksheet summarizes the total MLPs used as a percentage of the total available MLPs present in the device. It also shows the sum of instance and interconnect power as the total dynamic power dissipation from MLP usage based on the user-specified inputs and highlights it as a percentage of the total dynamic power. This worksheet also shows the corresponding total dynamic current for the chosen CORE_VDD rail.

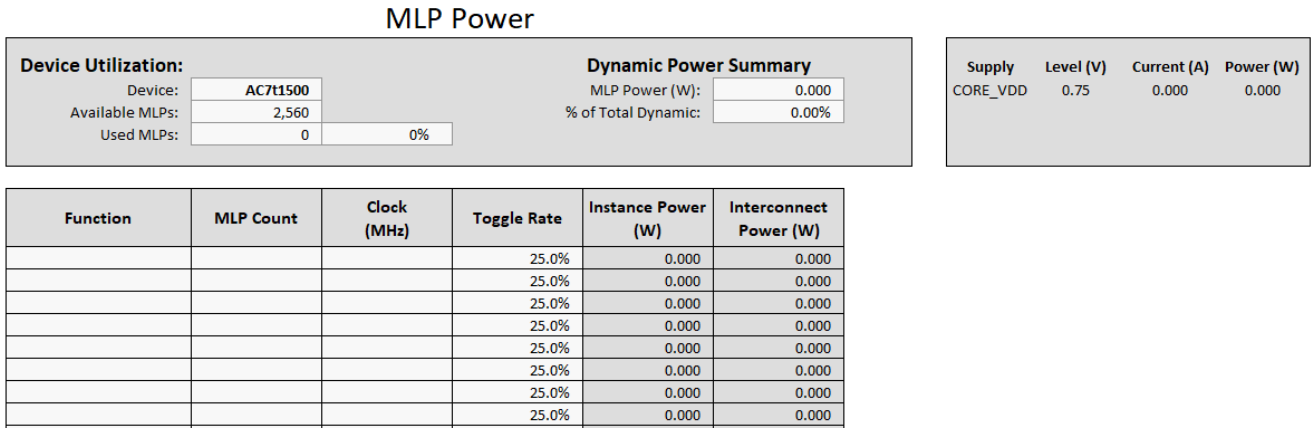


Figure 9: ***MLP Power Worksheet***

Table 6: ***MLP Power Worksheet Fields***

Input Parameter	Description
Input Fields	
Function	Description about the functionality/module associated with the MLP. This entry is optional.
MLP Count	The number of MLPs used in the function/module of the design.
Clock (MHz)	The clock frequency for the MLP used in this circuitry.
Toggle Rate	The percentage at which the MLP data toggles on each clock cycle for that module.
Calculated Fields	
Instance Power (W)	Calculation of the total power used by the MLPs for a particular function/module.
Interconnect Power (W)	Total dynamic power contributed by the interconnects to/from MLPs

NoC Worksheet

The network-on-chip (NoC) power worksheet summarizes the total dynamic power consumed by NoC resources specified by the user.

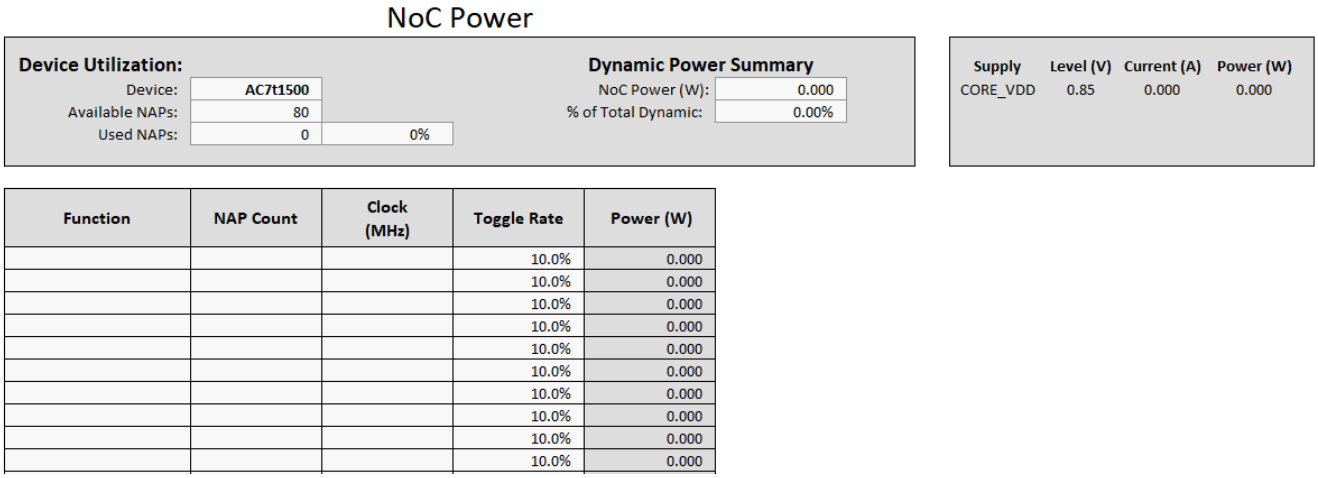


Figure 10: ***NoC Power Worksheet***

Table 7: ***NoC Power Worksheet Fields***

Input Parameter	Description
Input Fields	
Function	Description about the functionality/module associated with the NoC. This entry is optional.
NAP Count	The number of NoC access points (NAPs) used in the function/module of the design.
Clock (MHz)	The clock frequency for the NoC used in this circuitry.
Toggle Rate	The percentage at which the NoC data toggles on each clock cycle for that module.
Calculated Fields	
Power (W)	The total dynamic power used by the NoCs for a particular function/module.

I/O Worksheet

The I/O power worksheet provides the user a summary of the total dynamic power consumed by the total I/O utilization and a breakdown of each of the I/O power rails based on the I/O standard selection. The worksheet also presents the I/O utilization percentage for each I/O type used.

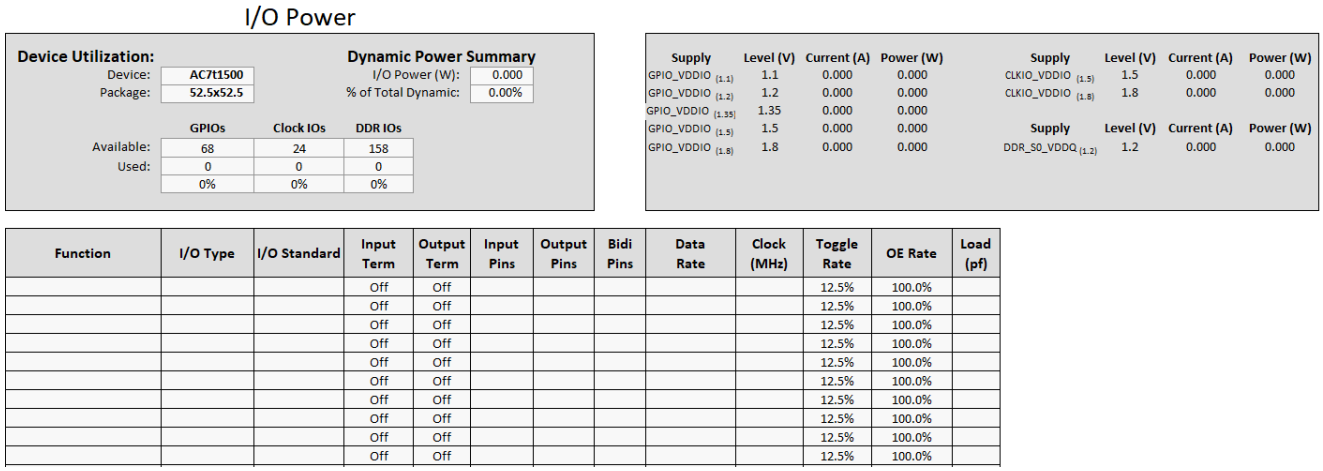


Figure 11: *I/O Power Worksheet*

Table 8: *I/O Power Worksheet Fields*

Input Parameter	Description
Input Fields	
Function	Description about the functionality/module associated with the I/O type. This entry is optional.
I/O Type	The I/O type selection to indicate if the associated I/O are one of the following: GPIO/CLKIO/DDRIO. The DDRIO indicates the DDR IOs that are intended to be used as general-purpose I/O.
I/O Standard	The I/O standard selection from the list of supported standards.
Input Term	Input field to indicate if input termination is enabled in the I/O.
Output Term	Input field to indicate if output termination is enabled in the I/O.
Input Pins	Input field to indicate if the I/O pins are input pins.
Output Pins	Input field to indicate if the I/O pins are output pins.
Bidi Pins	Input field to indicate if the I/O pins are bidirectional pins.
Data Rate	Option to select if the data rate associated with the I/O is single data rate (SDR) or double data rate (DDR).
Clock (MHz)	The frequency in MHz at which the I/O operate.

Input Parameter	Description
Toggle Rate	Input field to indicate the rate at which the I/O pins toggle. The default rate is 12.5%.
OE Rate	Input field to indicate the rate at which the output of the I/O is enabled. The default rate is 100%.
Load (pF)	Input field to indicate the load capacitance of the I/O pin (in picofarads).

The resultant power estimates based on the entered input parameters is summarized based on the I/O type and standard selection along with the supply voltage and current consumption.

SerDes Worksheet

The SerDes power worksheet provides a summary of the total number of SerDes lanes used in the design versus the available number of lanes and the total dnamic power of the SerDes lanes used based on the following input parameters provided by the user. In addition, it also provides a breakdown of the total dynamic current for each SerDes voltage rail, SRDS_PA_VDDH and SRDS_PA_VDDL.

SerDes Power

Device Utilization:		Dynamic Power Summary	
Device:	AC7t1500	SerDes Power (W):	0.000
Package:	52.5x52.5	% of Total Dynamic:	0.00%
Available SerDes:	32		
Used SerDes:	0		
	0%		

Supply	Level (V)	Current (A)	Power (W)
SRDS_PA_VDDH	1.20	0.000	0.000
SRDS_PA_VDDL	0.75	0.000	0.000

Function	Bus Width	SerDes Mode	Rx / Tx Mode	Data Rate (Gbps)	Power(W)
Raw SerDes					
		PAM4	Tx and Rx		0.000
		PAM4	Tx and Rx		0.000
		PAM4	Tx and Rx		0.000
		PAM4	Tx and Rx		0.000
		PAM4	Tx and Rx		0.000
		PAM4	Tx and Rx		0.000
		PAM4	Tx and Rx		0.000
		PAM4	Tx and Rx		0.000
		PAM4	Tx and Rx		0.000
		PAM4	Tx and Rx		0.000
		PAM4	Tx and Rx		0.000
		PAM4	Tx and Rx		0.000
		PAM4	Tx and Rx		0.000
		PAM4	Tx and Rx		0.000
		PAM4	Tx and Rx		0.000
		PAM4	Tx and Rx		0.000
		PAM4	Tx and Rx		0.000
		PAM4	Tx and Rx		0.000
		PAM4	Tx and Rx		0.000
		PAM4	Tx and Rx		0.000
		PAM4	Tx and Rx		0.000
Hard IP based SerDes					
		PAM4	Tx and Rx		0.000
		PAM4	Tx and Rx		0.000
		PAM4	Tx and Rx		0.000

Figure 12: ***SerDes Power Worksheet***

Raw SerDes

The first section of the SerDes worksheet is dedicated to computing the dynamic power of the raw SerDes lanes used in the device. The user needs to provide the input parameters indicated in the table below in order for the tool to compute the dynamic power.

Table 9: ***SerDes Power Worksheet Fields***

Input Parameter	Description
Input fields	
Function	Description about the functionality/module associated with the SerDes. This entry is optional
Bus Width	The number of SerDes lanes used.
SerDes Mode	Selects the SerDes operation mode. Available modes are NRZ and PAM4.

Input Parameter	Description
Rx/Tx Mode	Option to select if the SerDes lanes operate in transmit mode, receive mode or both.
Data Mode (Gbps)	Input to specify the maximum rate of operation of the SerDes lanes in Gbps. The maximum supported rate is 112 Gbps
Calculated Fields	
Power (W)	Calculated dynamic power based on the input parameters specified.

Hard IP Based SerDes

This section of the SerDes worksheet lists the different SerDes configurations used by the Ethernet and PCIe Hard IP used in the design. Similar to the DDR4 Interface I/O section, this section is also auto-populated by the Hard IP worksheet based on the various Hard IP selected. The total reported dynamic power also accounts for these herd IP SerDes rails, so the user need not enter them again in the Raw SerDes section. An example screenshot of the auto-populated IP SerDes lanes is shown below:

Hard IP based SerDes					
Ethernet	8	PAM4	Tx and Rx	53.125	2.864
PCI Express x16	4	NRZ	Tx and Rx	32	1.330
Ethernet Shared	2	PAM4	Tx and Rx	53.125	0.716
		PAM4	Tx and Rx		0.000
		PAM4	Tx and Rx		0.000

Figure 13: ***Example of Auto-populated Hard IP Based SerDes***

PLL Worksheet

The PLL Power worksheet provides the total dynamic power consumed by the PLLs and also the percentage of the total number of PLLs used. This worksheet also presents a power breakdown for each general-purpose PLL and DDR PLL voltage supplies. The ENoC_PLL_VDDA corresponds to the power supply of the ENoC PLL. Similarly, the GCG_PLL_VDDA corresponds to the global clock generator PLL power supply and the DDR_S0_VAA to the DDR PLL supply.

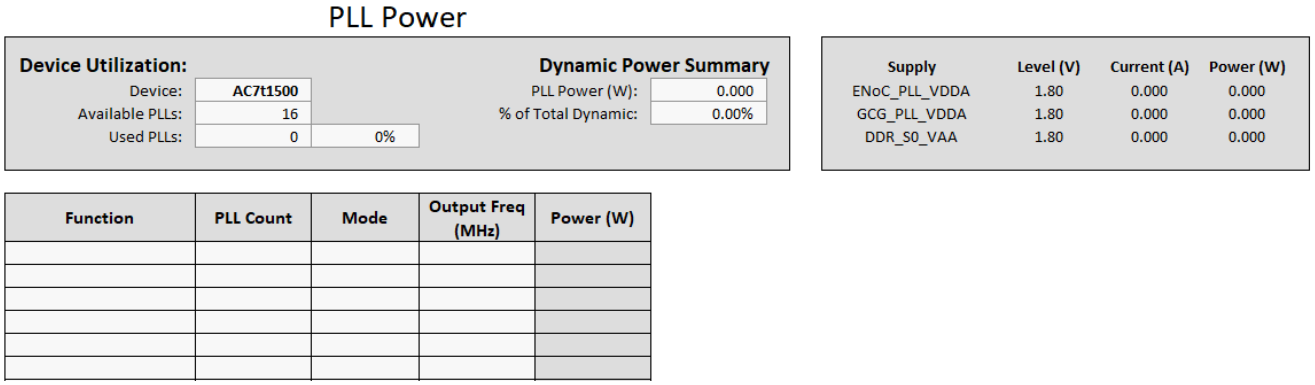


Figure 14: *PLL Power Worksheet*

Table 10: *PLL Power Worksheet Fields*

Input Parameter	Description
Input fields	
Function	Description about the functionality/module associated with the PLL. This entry is optional.
PLL Count	The number of PLLs used.
Mode	Allows the user to select the PLL type from one of the following options: ENoC, GCG, DDR.
Output Freq(MHz)	Input field to enter the PLL output frequency in MHz. Allowable range is 100 MHz to 4 GHz.
Calculated Fields	
Power (W)	Calculated dynamic power based on the input parameters specified.

Clock Worksheet

The clock power worksheet estimates the total dynamic power consumed by the clock network as a function of the utilization of DFFs, BRAMs, MLPs and LRAMs that contribute to the clock fanout.

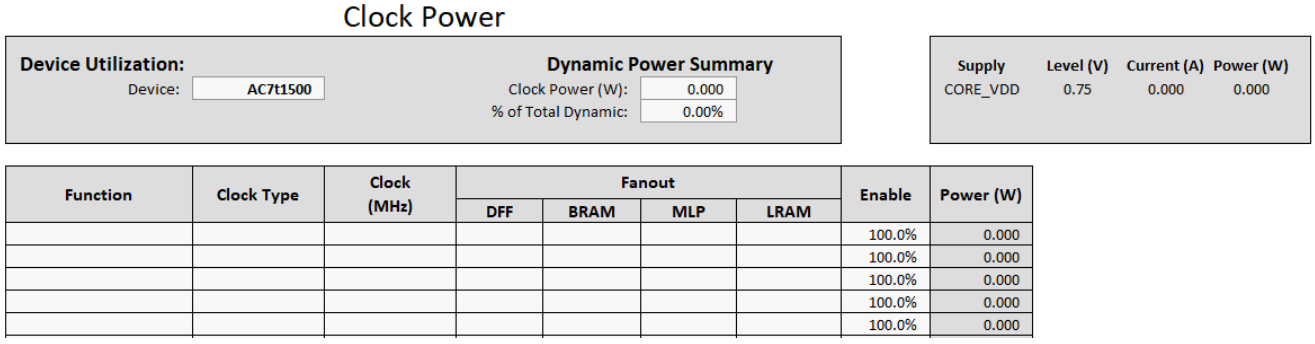


Figure 15: *Clock Power Worksheet*

Table 11: *Clock Power Worksheet Fields*

Input Parameter	Description
Input fields	
Function	Description about the functionality/module associated with the Clock. This entry is optional.
Clock Type	Option to indicate if the clock is a trunk, mini-trunk or branch clock.
Clock (MHz)	Input field to enter the clock frequency in MHz.
Fanout	The total fanout from the output of clock network to all registers including DFFs, BRAMs, LRAMs and MLPs. The user is required to enter the total DFFs, BRAMs, DSPs and LRAMs used in the design to compute the total fanout.
Enable	The percentage of time for which the clock is enabled.
Calculated Fields	
Power(W)	Calculated dynamic power based on the input parameters specified.

Hard IP Worksheet

The Hard IP power worksheet estimates the total dynamic power as a sum total of the dynamic power contributed by the various interfacing IP in Speedster7t FPGA and their percentage utilization. The total dynamic power is further broken down to provide the power consumed by each power supply of the associated hard IP and the corresponding current value.

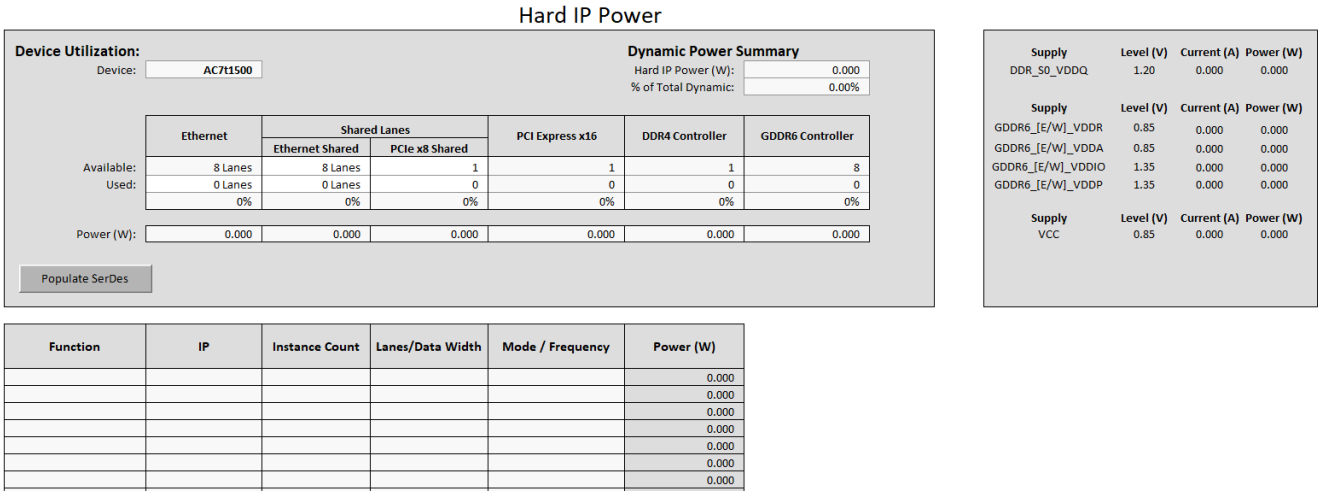


Figure 16: *Hard IP Power Worksheet*

Shared Lanes

The shared lanes column in the Hard IP worksheet denotes the second Ethernet IP and the PCIe ×8 interface that share the eight SerDes Lanes. These eight SerDes lanes can be used for any one of these interfaces at any given time. Hence, if the shared Ethernet IP is used, the PCIe ×8 utilization is automatically set to not being available and vice versa.

Populate SerDes

Once the user enters the different IP interfaces and configurations in the input filed, clicking this option will auto-populate the Hard IP SerDes section in the SerDes worksheet if there are any Ethernet or PCIe interfaces used. If any of the these entries are modified in the Hard IP worksheet, clicking this option again will update the corresponding entries in the SerDes worksheet

The following input fields are required to be entered by the user for each individual IP configuration used in the device.

Table 12: *Hard IP Worksheet Fields*

Input Parameter	Description
Input fields	
Function	Description about the functionality/module associated with each IP. This entry is optional.
IP	Selection to choose from a list of IP supported in the device.
Instance Count	Input field to indicate the number of the IP instances used.
Lanes/Data Width	Drop-down menu to choose the number of data lanes or data width for each IP. The drop-down option in this field varies for each IP selection.
Mode /Frequency	Drop-down menu to select the mode or operating frequency associated with each IP. The available options vary for each IP.
Calculated Fields	
Power (W)	Calculated dynamic power based on the input parameters specified.

Revision History

Version	Date	Description
1.0	13 Apr 2020	• Initial Achronix release.