Speedster7t Pin Connectivity User Guide (UG084)

Speedster FPGAs

Achronix
Data Acceleration

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Chapter 1 : Introduction

This user guide lists each of the I/O pin groups available in the Speedster® 7t700, 7t800, 7t1400, and 7t1500 FPGAs, their functionality and recommended connection guidelines.

Chapter 2 : Pin List and Connection Guidelines

This section contains the pin lists for each Speedster7t FPGA:

- AC7t1400/AC7t1500 (page 2)
- AC7t700/AC7t800 (page 11)

AC7t1400/AC7t1500

The following Table contains the updated recommended values of pull-up and pull-down impedance based on the Speedster7t 7t1500/7t1400 silicon.

Table 1 • AC7t1400/AC7t1500 Pin List

Pin Name	Type	Description and Connection Guidelines
Clock I/O Interface (15)		
CLKIO_NE_MSIO_[N/P]	Input/Output	A group of two clock buffers in each corner of the device. Can be used either as a single pseudo-differential clock I/O port or two single-ended clock I/O ports. Supported voltage levels are 1.5V and 1.8V. If not used as clock buffers, they can only be used as reset inputs. (1) • All the MSIO pins can be used to drive reset inputs to one of the interface subsystems, but *not* as reset to the core fabric. • The valid range of input and output clock frequency for MSIO pins is 0.75 to 500.0 MHz.
CLKIO_NW_MSIO_[N/P]		
CLKIO_SE_MSIO_[N/P]		
CLKIO_SW_MSIO_[N/P]		
CLKIO_NE_MSIO_ZCAL	Input	Impedance calibration inputs, one for each CLKIO bank. Common for both on-die termination and output drivers. For Tx, the ZCAL is used for output drivers and for Rx the on-die termination uses the ZCAL. (11)
CLKIO_NW_MSIO_ZCAL		
CLKIO_SE_MSIO_ZCAL		
CLKIO_SW_MSIO_ZCAL		

Pin Name	Type	Description and Connection Guidelines
CLKIO_NE_REFIO_[N/P]_0 (1)	Input/Output	A set of eight differential reference clock input/output pairs, two pairs in each corner of the device. If these pairs are not used as clock buffers, each REFIO pair can receive up to two reset inputs. The REFIO supports the following configurations: • Differential LVCMOS_18 and LVCMOS_15, LVDS_18 and LVDS_15, LVPECL. Can have an input frequency range from 5 MHz to 600 MHz when supplied as the input reference clock to the PLL and in internal PLL bypass mode. In external PLL bypass mode, the maximum input frequency is up to 1 GHz. • As outputs, the REFIO interfaces can clock from 10 MHz up to 1 GHz. • All the REFIO pins can be used to drive reset inputs to the interface subsystems. **Note** • The LVPECL I/O must be AC coupled on the board • Only pins CLKIO_NE/NW_REFIO_P_0 can be used to drive resets to the core fabric
CLKIO_NE_REFIO_[N/P]_1		
CLKIO_NW_REFIO_[N/P]_0		
CLKIO_NW_REFIO_[N/P]_1		
CLKIO_SE_REFIO_[N/P]_0		
CLKIO_SE_REFIO_[N/P]_1		
CLKIO_SW_REFIO_[N/P]_0		
CLKIO_SW_REFIO_[N/P]_1		
CLKIO_NE_VREF	Input	Optional external reference voltage supply to the CLKIO, typically set to CLKIO_*_VDDIO/2 when supplied externally. When this voltage is internally supplied by the CLKIO macro, these pins should be connected to ground.
CLKIO_NW_VREF		
CLKIO_SE_VREF		
CLKIO_SW_VREF		
IEEE1149.1/1149.6 JTAG Interface (10, 16)		
JTAG_TCK	Input	JTAG test clock. Dedicated test clock advances the TAP controller and clocks data in on the TDI input and out on the TDO output. The maximum frequency for TCK is 50 MHz.
JTAG_TDI	Input	JTAG test data in. Serial instruction and test data input. Data is captured on the rising edge of the test logic clock (TCK).
JTAG_TDO	Output	JTAG test data out. Serial data from test logic output. TDO is set to an inactive drive state (high impedance) when data scanning is not in progress. TDO valid data is output on the falling edge of TCK.
JTAG_TMS	Input	JTAG test mode select. Controls the test access port (TAP) controller state machine transitions. Captured on the rising edge of TCK.
JTAG_TRSTN	Input	JTAG test reset. Active-low reset input initializes the TAP controller.
Configuration Interface(16)		
FCU_CONFIG_BYPASS_CLEAR (2)	Input	Active-high input pin bypasses configuration memory clear during device initialization. Should be tied to GND if not used. The recommended pull-down impedance is 10 KΩ and recommended pull-up impedance is 100Ω.

Pin Name	Type	Description and Connection Guidelines
FCU_CONFIG_CLKSEL (2)	Input	Controlling whether the FPGA configuration unit (FCU) clock is sourced from the TCK input or the CPU_CLK input (see FCU Configuration Clock Selection (page 20)). This pin should be connected to a configurable input such as a DIP switch to toggle between modes of operation for debug. If this is not possible or desired, tie this signal to 1.8V (FCU_CB_VDDIO) or GND based on the desired clock for configuration mode. To achieve a default digital '0' or '1', weak pull down/up of 1 KΩ is recommended. To toggle the pin from its default state, stronger pull up/down will have to be provided either through a jumper plus pull up/down resistor (~100Ω) or through an on-board GPIO to drive the signal to 1/0.
FCU_CONFIG_ERR_ENC[2:0]	Output	Active-high output pins highlighting the presence of CRC, scrubbing or other errors in the bitstream during device programming. If asserted, remains high, in which case, expect configuration loading to never complete, and user mode is never entered (see Bitstream Programming Error Output Pins Messages (page 20)). Connect these pins directly to an error indicator. Its recommended to use a pull-down impedance of 1 KΩ to avoid accidental triggering of these pins to high digital state.
FCU_CONFIG_DONE (14)	Input(22)/Output	Configuration done output signal. A high indicates bitstream loading completed successfully and the device is ready to enter user mode. If a device configuration error occurs, CONFIG_DONE remains low. This pin must be held low to synchronize the start-up of multiple devices. Must be kept high at power up to digital '1' as the FCU can only trigger configuration when this pin is logic '1'. Recommended pull-up impedance is 10 KΩ.
FCU_CONFIG_MODESEL[3:0] (2)	Input	Configuration mode selection inputs to define FCU mode of operation (see MODESEL Pins FCU Mode Selection (page 21)). Should be connected to configurable inputs such as DIP switches to toggle between modes of operation for debug. If this is not possible or desired based on the configuration scheme, tie to either FCU_CB_VDDIO or GND using a pull-up/pull-down resistor. To achieve a default digital '0' or '1', weak pull down/up of 1 KΩ is recommended. To toggle the pin from its default state, stronger pull up/down will have to be provided either through a jumper + pull up/down resistor (~100Ω) or through an on-board GPIO to drive the signal to 1/0.
FCU_PARTIAL_CONFIG_DONE	Input(22)/Output	Active-high, open-drain configuration done output signal indicating bitstream loading completed successfully for partial device reconfiguration, and device is ready to enter user mode. Connect this output directly to an indicator LED or configuration controller. Must be kept high at power up to digital '1' as the FCU can only trigger configuration when this pin is logic '1'. Recommended minimum pull-up impedance is 10 KΩ.
FCU_CONFIG_RSTN (3)	Input	Asynchronous active-low reset input clears the device configuration memory and FCU logic. During device power-up, this pin must be held low and must not have any glitch. All other input pins must be stable when FCU_CONFIG_RSTN is ready to be released after power-up. Recommended pull-up impedance is 100 KΩ.

Pin Name	Type	Description and Connection Guidelines
FCU_STRAP[2:0]	Input	Test mode input pins. When FCU_STRAP[0] is 0, FCU is in functional mode and, when 1, FCU_CPU_CSN is gated and only controllable via test logic. Pins must be enabled with a provision to connect pull-down resistors in order to drive the appropriate input value. Recommended pull-down impedance is 1 KΩ.
FCU_STAP_SEL (2)	Input	When high, enables the JTAG interface pins to be directly connected to the JTAG controller in the SerDes PMA blocks allowing for SerDes configuration, debug and performance monitoring directly from the JTAG interface. For bitstream download and design debug using the JTAG interface, must be held low. For SerDes PMA debug only mode, must be held high. Must be connected to a configurable input, such as a DIP switch, to toggle between modes of operation for debug. Recommended pull-down impedance is 1 KΩ. If pin is not used, should be tied to GND using a pull-down resistor.
FCU_CONFIG_STATUS (14)	Input(22)/Output	Active-high configuration status open-drain output signal indicates FCU has completed initial start-up, has cleared the CMEM and is awaiting FCU commands for bitstream programming. When high, the signal remains asserted until FCU is power cycled, reset for a re-initialization sequence, or a CRC error is seen during bitstream load. The recommended minimum pull-up impedance is 10 KΩ.
FCU_CONFIG_SYSCLK_BYPASS (2)	Input	Active-high setting bypasses configuration system clock. Along with CFG_CLKSEL, this setting allows clock selection during programming (see FCU Configuration Clock Selection (page 20)). Should be connected to a configurable input, such as a DIP switch, to toggle between modes of operation for debug. If not possible or desired, tie to 1.8V (FCU_CB_VDDIO) or GND based on desired clock for configuration mode. Recommended pull-down impedance is 1 KΩ.
FCU_CONFIG_USER_MODE	Output	Active-high output indicating that the device has transitioned into user mode. When high, remains asserted until the FCU is power-cycled or reset for a re-initialization sequence. Not an open drain output. Can be connected directly to an indicator LED or configuration controller. The recommended pull-down impedance is 1 KΩ.
FCU_CPU_CLK	Input	Input clock from external CPU. The data/address bus is synchronous to this clock. If the CPU_CLK is not used to source the FCU clock, should be tied to GND. Must operate at 100 MHz when programming any design bitstream using the Achronix device manager. Recommended pull-down impedance is 10 KΩ.
FCU_CPU_CSN	Input	Active-low CPU mode chip select. Connect directly to the configuration controller. If not used, should be connected to a pull-up resistor. Recommended pull-up impedance value is 10 KΩ.
FCU_CPU_DQ_IN_OUT[31:0] (3)	Input/Output	Data input/output pins shared between the CPU and flash interfaces. CPU interface is inaccessible when flash mode in use and vice-versa. If any pins are unused based on the configuration, they should connect to weak pull-up resistors.
FCU_CPU_DQ_VALID (3)	Output	Active-high control bit indicates to CPU on which clock cycles the CPU_DQ bus has valid read-back data. Synchronous to FCU_CPU_CLK.

Pin Name	Type	Description and Connection Guidelines
FCU_LOCK (3)	Output	Active-high status bit indicates FCU lock/unlock status. Recommended pull-down impedance is 1 KΩ.
FCU_STATUS[1:0] (3)	Output	FCU status bits showing the FCU state. Bits are detailed in FCU_STATUS Bits Indicating FCU State (page 21).
FCU_FLASH_CSN[3:0]	Output	Active-low chip select enables/disables one or more attached flash memory devices: • For ×1 mode, only CSN[0] is used. Unused CSN[3:1] pins must be tied high. • For ×4 mode, each CSN[3:0] connects to a flash device. Connect all four to individual signals of serial flash devices.
FCU_FLASH_HOLDN (3)	Output	Active-low hold output to flash memory device(s). Pauses serial communications between the FPGA and flash device without deselecting the device or stopping the serial clock. Synchronous to FLASH_SCK.
FCU_FLASH_SCK	Output	Clock output from FCU to flash memory device(s). Connect directly to the flash device(s).
FCU_OSC_CLK (3)	Output	This clock is internally generated from a ring oscillator. For debug purposes, can be bypassed, and external clock CPU_CLK can be used.
General Purpose I/O Interface(17)		
GPIO_[N0/S0]_BYTE[2:0]_VREF	Input	Optional external reference voltage supply to GPIO. Typically connected to GPIO_VDDIO/2 when supplied externally. When voltage is supplied internally by MSIO macro, should be connected to ground.
GPIO_[N0/S0]_ZCAL (11)	Input	Impedance calibration input, one for each GPIO bank, common for both on-die termination and output driver.
GPIO_[N0/S0]_BYTE[1:0]_BIT_[11:0] (1)	Input/Output	Single-ended GPIO ports supporting multiple I/O standards at multiple voltages. Bytes 0 and 1 contain a group of 12 I/O pins out of which ten are dedicated to data and two are dedicated to clock. Byte 2 has a group of eight I/O pins out of which six are dedicated to data and two are dedicated to clock. Pseudo-differential pairs can be built using two adjacent buffers.
GPIO_[N0/S0]_BYTE2_BIT_[7:0]		
SerDes(18)		
PCIe_x16		
SRDS_N03_ATEST (13)	Output	High-impedance output pin to probe multiplexed internal analog nodes during system bring-up.
SRDS_N[3:0]_REFCLK_[N/P] (6) (12)	Input	SerDes reference clock supplied from differential external source. There is a single differential pair for each quad. Each SerDes quad has a common reference clock.
SRDS_N[3:0]_RX_[N/P][3:0] (5)	Input	SerDes receive differential inputs, one differential pair per lane.

Pin Name	Type	Description and Connection Guidelines
SRDS_N[3:0]_TX_[N/P][3:0] (4)	Output	SerDes differential Transmit outputs, one differential pair per lane.
Ethernet(19)		
SRDS_N47_ATEST (13)	Output	High-impedance output pin probes/forces internal analog nodes during system bring-up.
SRDS_N[5:4]_REFCLK_[N/P] (6) (12)	Input	SerDes reference clock supplied from either single-ended or differential external source. Single differential pair per quad.
SRDS_N[5:4]_RX_[N/P][3:0] (5)	Input	Receive differential inputs to the SerDes. One differential pair per lane.
SRDS_N[5:4]_TX_[N/P][3:0] (4)	Output	SerDes transmit differential outputs. One differential pair per lane.
Shared PCIe_x8 and Ethernet		
SRDS_N[7:6]_REFCLK_[N/P] (6)	Input	SerDes reference clock supplied from either single-ended or differential external source. One differential pair per quad. If SerDes configured to be in PCIe ×8 mode, reference clocks for both SerDes quads must be connected.
SRDS_N[7:6]_RX_[N/P][3:0] (5)	Input	SerDes receive differential inputs. One differential pair per lane.
SRDS_N[7:6]_TX_[N/P][3:0] (4)	Output	SerDes transmit differential outputs. One differential pair per lane.
Miscellaneous		
TS_AN_IO_[1:0]	Input/Output	Analog I/O pins for test access and calibration. For internal temperature calibration purposes only. Leave unconnected.
DDR4 (9, 20)		
DDR4_S0_A17 (7)	Output	SDRAM address input (used in ×4 configuration only).
DDR4_S0_ACT_N (7)	Output	SDRAM active-low ACTIVATE command.
DDR4_S0_A_[13:0] (7)	Output	SDRAM bank address inputs.
DDR4_S0_BA_[1:0] (7)	Output	SDRAM bank select inputs.
DDR4_S0_BG_[1:0] (7)	Output	SDRAM bank group inputs.
DDR4_S0_BP_ALERT_N (7)	Input/Output	DDR4 SDRAM I/O signal to the host controller indicating when the SDRAM detects an error on the DDR interface, or host controller a signal to the SDRAM during connectivity test mode.
DDR4_S0_BP_MEMRESET_L (7)	Output	Active-low external SDRAM memory reset signal.
DDR4_S0_BP_VREF (7)	Input/Output	External SDRAM reference voltage.

Pin Name	Type	Description and Connection Guidelines
DDR4_S0_BP_ZN	Output	External calibration reference resistor. Supported values are 40Ω, 120Ω and 240Ω ±1%.
DDR4_S0_CAS_N [7]	Output	External SDRAM active-low column address select signal. When ACT_N and CS_N are low, outputs are interpreted as column address bits. When ACT_N is high, outputs are interpreted as command pins indicating READ, WRITE or other commands.
DDR4_S0_CID_[2:0] [7]	Output	Stacked components chip ID select. Not applicable, since stacked devices are not supported for Speedster devices, but can still be used for DDR bypass mode.
DDR4_S0_CKE_[3:0] [7]	Output	SDRAM clock enable control signal.
DDR4_S0_CK_[N/P]_[3:0] [7]	Output	SDRAM differential clock inputs. All address, command, and control input signals are sampled on positive edge of CK_T and negative edge of CK_C.
DDR4_S0_CS_N_[3:0] [7]	Output	External SDRAM active-low chip select signals. All commands are masked when CS_n is registered high. CS_N provides external rank selection on systems with multiple ranks.
DDR4_S0_UDQS_N_[8:0] [7]	Input/Output	SDRAM data strobe signals.
DDR4_S0_DQ_[8:0]_[7:0] [7]	Input/Output	SDRAM data bus.
DDR4_S0_LDQS_[N/P]_[8:0] [7]	Input/Output	SDRAM data strobe signals.
DDR4_S0_ODT_[3:0] [7]	Output	SDRAM on-die termination control signal. ODT resistances can be configured to one of open, 240, 120, 80, 60, 48 or 40Ω pulled up to DDR4_S0_VDDQ (refer to SDRAM device datasheet).
DDR4_S0_PAR [7]	Output	Command/address parity input to the SDRAM.
DDR4_S0_RAS_N [7]	Output	External SDRAM active-low row address select signal. When ACT_N and CS_N are low, these outputs are interpreted as row address bits. When ACT_N is high, these outputs are interpreted as command pins indicating READ, WRITE or other commands.
DDR4_S0_DM_DBI_UDQS_P_[8:0] [7]	Input/Output	SDRAM data mask and data bus inversion signals.
DDR4_S0_WE_N [7]	Output	Active-low write enable signal.
GDDR6 [21]		
GDDR6_[E/W][3:0]_C[1:0]_SD_CABI_N [8]	Output	GDDR6 memory active-low command address bus inversion input.
GDDR6_[E/W][3:0]_C[1:0]_SD_CA_[9:0] [8]	Output	GDDR6 memory command address inputs.
GDDR6_[E/W][3:0]_C[1:0]_SD_CKE_N [8]	Output	GDDR6 memory active-low clock enable input.

Pin Name	Type	Description and Connection Guidelines
GDDR6_[E/W][3:0]_C[1:0]_SD_DBI_N_[1:0] (8)	Input/Output	GDDR6 memory active-low data bus inversion inputs.
GDDR6_[E/W][3:0]_C[1:0]_SD_DQ_[15:0] (8)	Input/Output	Bidirectional data input/output.
GDDR6_[E/W][3:0]_C[1:0]_SD_EDC_[1:0] (8)	Input	GDDR6 memory error detection code.
GDDR6_[E/W][3:0]_C[1:0]_SD_WCK_[N/P]_[1:0] (8)	Output	Memory differential data clock inputs.
GDDR6_[E/W] [3:0]_RREF	Input	ZQ calibration reference resistor. Nominal 240Ω resistance to ground, ±1% tolerance.
GDDR6_[E/W] [3:0]_SD_CLK_[N/P] (8)	Output	Differential memory clock inputs.
GDDR6_[E/W] [3:0]_SD_RESET_N (8)	Output	GDDR6 memory active-low reset.
GDDR6_E2_ATESTCA (13)	Input	CA signals analog voltage monitor.
GDDR6_E2_ATESTDQL (13)	Input	Lower DQ signals analog voltage monitor.
GDDR6_E2_ATESTDQR (13)	Input	Higher DQ signals analog voltage monitor.
GDDR6_W1_ATESTCA (13)	Input	CA signals analog voltage monitor.
GDDR6_W 1_ATESTDQL (13)	Input	Lower DQ signals analog voltage monitor.
GDDR6_W 1_ATESTDQR (13)	Input	CA signals analog voltage monitor.

Pin Name	Type	Description and Connection Guidelines

Table Notes

1. Unused I/O can be left unconnected.
2. Do not leave specified pin(s) unconnected.
3. Connect directly to the configuration controller.
4. These pins should be AC coupled. Leave all unused transmit pins unconnected.
5. Leave all unused receive pins unconnected.
6. Connect individual reference clocks for all SerDes quads used in the interface. Optionally, forward a reference clock for one quad to the neighboring quads by selecting **Enable PMA Ref Clock Sharing** in the SerDes IP configuration editor. Tie the unused quads reference clocks to their own individual GND via an optional 50Ω ±1% termination resistor.
7. Connect to the appropriate signals on the DDR4 DIMM.
8. Connect to the appropriate GDDR6 memory signals. If, the GDDR interface is not used, the I/O can be left floating.
9. If the DDR4 interface is not used, the DDR PHY can be set in bypass mode where the unused DDR4 I/O can be used as special-purpose I/O for low-speed applications such as boundary scan, DC I/O parametric testing, SoC-level ATPG I/O and DDR4 memory connectivity testing. The direction of these pins is retained from that of the DDR4 interface. All DDR I/O pins may either be used as special-purpose I/O or the entire set may be used for DDR4 interfacing, but a combination of both is not allowed. If DDR pins are not used at all, they can be left floating.
10. The JTAG interface pins should be brought out to a JTAG header on the board (the connections must adhere to the JTAG interface standard). These JTAG pins should never be left unconnected and should be connected to a JTAG header even when not used.
11. Requires an off-chip ±1% precision 240Ω resistor terminated to ground.
12. Unused clocks should be tied to their own individual GND via an optional 50Ω ±1% precision termination resistor.
13. Connect directly to observation point.
14. This output is an open-drain signal. In the default mode of operation, it is recommended that this signal be connected to an LED as an indicator on the board.
15. More details about the clock I/O interface can be found in the *Speedster7t Clock and Reset Architecture User Guide* (UG083)[1].
16. More details about the JTAG and configuration interface can be found in the *Speedster7t Configuration User Guide* (UG094)[2].
17. More details about the GPIO interface can be found in the *Speedster7t GPIO User Guide* (UG112)[3].
18. More details about the serdes interface can be found in the *Speedster7t SerDes User Guide* (UG099)[4].
19. More details about the ethernet interface can be found in the *Speedster7t Ethernet User Guide* (UG097)[5].
20. More details about the DDR interface can be found in the *Speedster7t DDR User Guide* (UG096)[6].
21. More details about the GDDR6 interface can be found in the *Speedster7t GDDR6 User Guide* (UG091)[7].
22. Input is reserved for internal status monitoring only.

1 https://www.achronix.com/documentation/speedster7t-clock-and-reset-architecture-user-guide-ug083
2 https://www.achronix.com/documentation/speedster7t-configuration-user-guide-ug094
3 https://www.achronix.com/documentation/speedster7t-gpio-user-guide-ug112
4 https://www.achronix.com/documentation/speedster7t-serdes-user-guide-ug099
5 https://www.achronix.com/documentation/speedster7t-ethernet-user-guide-ug097
6 https://www.achronix.com/documentation/speedster7t-ddr-user-guide-ug096
7 https://www.achronix.com/documentation/speedster7t-gddr6-user-guide-ug091

AC7t700/AC7t800

The following Table contains the updated recommended values of pull-up and pull-down impedance based on the Speedster7t 7t800 silicon.

Table 2 • AC7t700/AC7t800 Pin List

Pin Name	Type	Description and Connection Guidelines
Clock I/O Interface[15]		
CLKIO_0_MSIO_[N/P] CLKIO_1_MSIO_[N/P]	Input/ Output	A group of two clock buffers in each corner of the device. Can be used either as a single pseudo-differential clock I/O port or two single-ended clock I/O ports. Supported voltage levels are 1.5V and 1.8V. If not used as clock buffers, they can only be used as reset inputs. [1] • All the MSIO pins can be used to drive reset inputs to the interface subsystems or the core fabric. Up to four resets from all CLKIO sources may be driven to the core. • The valid range of input and output clock frequency for MSIO pins is 0.75 to 500.0 MHz.
CLKIO_0_MSIO_ZCAL CLKIO_1_MSIO_ZCAL	Input	Impedance calibration inputs, one for each CLKIO bank. Common for both on-die termination and output drivers. For Tx, the ZCAL is used for output drivers and for Rx the on-die termination uses the ZCAL. [11]
CLKIO_0_REFIO_[N/P]_0 [1] CLKIO_0_REFIO_[N/P]_1 CLKIO_1_REFIO_[N/P]_0 CLKIO_1_REFIO_[N/P]_1	Input/ Output	A set of eight differential reference clock input/output pairs, two pairs in each corner of the device. If these pairs are not used as clock buffers, each REFIO pair can receive up to two reset inputs. The REFIO supports the following configurations: • Differential LVCMOS_18 and LVCMOS_15, LVDS_18 and LVDS_15, LVPECL. Can have an input frequency range from 5 MHz to 600 MHz when supplied as the input reference clock to the PLL and in internal PLL bypass mode. In external PLL bypass mode, the maximum input frequency is up to 1 GHz. • As outputs, the REFIO interfaces can clock from 10 MHz up to 1 GHz. • All the REFIO pins can be used to drive reset inputs to the interface subsystems. Additionally, any/all of the REFIO pins can drive reset inputs to the core fabric. Up to four resets from all CLKIO sources may be driven to the core. **Note** • The LVPECL I/O must be AC coupled on the board
CLKIO_0_VREF CLKIO_1_VREF	Input	Optional external reference voltage supply to the CLKIO, typically set to CLKIO_*_VDDIO/2 when supplied externally. When this voltage is internally supplied by the CLKIO macro, these pins should be connected to ground.
IEEE1149.1/1149.6 JTAG Interface [10, 16]		
JTAG_TCK	Input	JTAG test clock. Dedicated test clock advances the TAP controller and clocks data in on the TDI input and out on the TDO output. The maximum frequency for TCK is 50 MHz.
JTAG_TDI	Input	JTAG test data in. Serial instruction and test data input. Data is captured on the rising edge of the test logic clock (TCK).
JTAG_TDO	Output	JTAG test data out. Serial data from test logic output. TDO is set to an inactive drive state (high impedance) when data scanning is not in progress. TDO valid data is output on the falling edge of TCK.

Pin Name	Type	Description and Connection Guidelines
JTAG_TMS	Input	JTAG test mode select. Controls the test access port (TAP) controller state machine transitions. Captured on the rising edge of TCK.
JTAG_TRSTN	Input	JTAG test reset. Active-low reset input initializes the TAP controller.
Configuration Interface(16)		
FCU_CONFIG_BYPASS_CLEAR (2)	Input	Active-high input pin bypasses configuration memory clear during device initialization. Should be tied to GND if not used. The recommended minimum pull-down impedance is 10 KΩ and recommended pull-up impedance is 100Ω.
FCU_CONFIG_CLKSEL (2)	Input	Controlling whether the FPGA configuration unit (FCU) clock is sourced from the TCK input or the CPU_CLK input (see FCU Configuration Clock Selection (page 20)). Should be connected to a configurable input such as a DIP switch to toggle between modes of operation for debug. If this is not possible or desired, tie this signal to 1.8V (FCU_CB_VDDIO) or GND based on the desired clock for configuration mode. The recommended minimum pull-down impedance is 1 KΩ.
FCU_CONFIG_ERR_ENC[2:0]	Output	Active-high output pins highlighting the presence of CRC, scrubbing or other errors in the bitstream during device programming. If asserted, remains high, in which case, expect configuration loading to never complete, and user mode is never entered (see Bitstream Programming Error Output Pins Messages (page 20)). Connect these pins directly to an error indicator. The recommended minimum pull-down impedance is 1 KΩ.
FCU_CONFIG_DONE (14)	Input/ Output	Active-high, open-drain configuration done output signal indicating bitstream loading completed successfully and the device is ready to enter user mode. When high, the signal remains asserted until FCU is power-cycled or reset for a re-initialization sequence. If a device configuration error occurs, CONFIG_DONE remains low. This pin must be held low to synchronize the start-up of multiple devices. Also, must be tied high (even if not externally driven) as the FCU only proceeds when a high value is present. Recommended minimum pull-up impedance is 10 KΩ.
FCU_CONFIG_MODESEL[3:0] (2)	Input	Configuration mode selection inputs to define FCU mode of operation (see MODESEL Pins FCU Mode Selection (page 21)). Should be connected to configurable inputs such as DIP switches to toggle between modes of operation for debug. If this is not possible or desired based on the configuration scheme, tie to either FCU_CB_VDDIO or GND using a pull-up/pull-down resistor. Recommended pull-down resistor value is 1 KΩ.
FCU_PARTIAL_CONFIG_DONE	Input/ Output	Active-high, open-drain configuration done output signal indicating bitstream loading completed successfully for partial device reconfiguration, and device is ready to enter user mode. Connect this output directly to an indicator LED or configuration controller. Must be tied high (even if not externally driven) as the FCU only proceeds when a high value is present. Recommended minimum pull-up impedance is 10 KΩ.
FCU_CONFIG_RSTN (3)	Input	Asynchronous active-low reset input clears the device configuration memory and FCU logic. Must be held low, and cannot glitch during device power-up. All other input pins must be stable when `i_config_rstn` is ready to be released after power-up. Recommended minimum pull-up impedance is 100 KΩ.
FCU_STRAP[2:0]	Input	Test mode input pins. When FCU_STRAP[0] is 0, FCU is in functional mode and, when 1, FCU_CPU_CSN is gated and only controllable via test logic. Pins must be enabled with a provision to connect pull-down resistors in order to drive the appropriate input value. Recommended minimum pull-down impedance is 1 KΩ.
FCU_STAP_SEL (2)	Input	When high, enables the JTAG interface pins to be directly connected to the JTAG controller in the SerDes PMA blocks allowing for SerDes configuration, debug and performance monitoring directly from the JTAG interface. For bitstream download and design debug using the JTAG interface, must be held low. For SerDes PMA debug only mode, must be held high. Must be connected to a configurable input, such as a DIP switch, to toggle between modes of operation for debug. Recommended minimum pull-down impedance is 1 KΩ. If pin is not used, should be tied to GND using a pull-down resistor.

Pin Name	Type	Description and Connection Guidelines
FCU_CONFIG_STATUS (14)	Input/ Output	Active-high configuration status open-drain output signal indicates FCU has completed initial start-up, has cleared the CMEM and is awaiting FCU commands for bitstream programming. When high, the signal remains asserted until FCU is power cycled, reset for a re-initialization sequence, or a CRC error is seen during bitstream load. The recommended minimum pull-up impedance is 10 KΩ.
FCU_CONFIG_SYSCLK_BYPASS (2)	Input	Active-high setting bypasses configuration system clock. Along with CFG_CLKSEL, this setting allows clock selection during programming (see FCU Configuration Clock Selection (page 20)). Should be connected to a configurable input, such as a DIP switch, to toggle between modes of operation for debug. If not possible or desired, tie to 1.8V (FCU_CB_VDDIO) or GND based on desired clock for configuration mode. Recommended minimum pull-down impedance is 1 KΩ.
FCU_CONFIG_USER_MODE	Output	Active-high output indicating that the device has transitioned into user mode. When high, remains asserted until the FCU is power-cycled or reset for a re-initialization sequence. Not an open drain output. Can be connected directly to an indicator LED or configuration controller. The recommended minimum pull-down impedance is 1 KΩ.
FCU_CPU_CLK	Input	Input clock from external CPU. The data/address bus is synchronous to this clock. If the CPU_CLK is not used to source the FCU clock, should be tied to GND. Must operate at 100 MHz when programming any design bitstream using the Achronix device manager. Recommended minimum pull-down impedance is 10 KΩ.
FCU_CPU_CSN	Input	Active-low CPU mode chip select. Connect directly to the configuration controller. If not used, should be connected to a pull-up resistor. Recommended pull-up impedance value is 10 KΩ.
FCU_CPU_DQ_IN_OUT[7:0] (3)	Input/ Output	Data input/output pins shared between the CPU and flash interfaces. CPU interface is inaccessible when flash mode in use and vice-versa. If any pins are unused based on the configuration, they should connect to weak pull-up resistors.
FCU_CPU_DQ_VALID (3)	Output	Active-high control bit indicates to CPU on which clock cycles the CPU_DQ bus has valid read-back data. Synchronous to FCU_CPU_CLK.
FCU_LOCK (3)	Output	This pin is set high when stage0 bitstream programming is complete.
FCU_STATUS[1:0] (3)	Output	FCU status bits showing the FCU state. Recommended minimum pull-down impedance is 1 KΩ. Bits are detailed in FCU_STATUS Bits Indicating FCU State (page 21).
FCU_FLASH_CSN[3:0]	Output	Active-low chip select enables/disables one or more attached flash memory devices: • For ×1 mode, only CSN[0] is used. Unused CSN[3:1] pins must be tied high. • For ×4 mode, each CSN[3:0] connects to a flash device. Connect all four to individual signals of serial flash devices.
FCU_FLASH_HOLDN (3)	Output	Active-low hold output to flash memory device(s). Pauses serial communications between the FPGA and flash device without deselecting the device or stopping the serial clock. Synchronous to FLASH_SCK. If used, should be connected to a weak pull-up resistor.
FCU_FLASH_SCK	Output	Clock output from FCU to flash memory device(s). Connect directly to the flash device(s).
FCU_OSC_CLK (3)	Output	This clock is internally generated from a ring oscillator. For debug purposes, can be bypassed, and external clock CPU_CLK can be used.
General Purpose I/O Interface(17)		
GPIO_0_BYTE[1:0]_VREF	Input	Optional external reference voltage supply to GPIO. Typically connected to GPIO_VDDIO/2 when supplied externally. When voltage is supplied internally by MSIO macro, should be connected to ground.

Pin Name	Type	Description and Connection Guidelines
GPIO_[1:2]_VREF	Input	Optional external reference voltage supply to GPIO. Typically connected to GPIO_VDDIO/2 when supplied externally. When voltage is supplied internally by MSIO macro, should be connected to ground.
GPIO_[2:0]_ZCAL (11)	Input	Impedance calibration input, one for each GPIO bank, common for both on-die termination and output driver.
GPIO_0_BYTE[1:0]_BIT_[11:0] (1)	Input/ Output	Single-ended GPIO ports supporting multiple I/O standards at multiple voltages. Bytes 0 and 1 contain a group of 12 I/O pins out of which ten are dedicated to data and two are dedicated to clock. Byte 2 has a group of eight I/O pins out of which six are dedicated to data and two are dedicated to clock. Pseudo-differential pairs can be built using two adjacent buffers.
GPIO_[1:2]_[25:0]		
SerDes(18)		
PCIe_x16		
SRDS_03_ATEST (13)	Output	High-impedance output pin to probe/force internal analog nodes during system bring-up.
SRDS_[3:0]_REFCLK_[N/P] (6) (12)	Input	SerDes reference clock supplied from either single-ended or differential external source. There is a single differential pair for each quad. Each SerDes quad has a common reference clock.
SRDS_[3:0]_RX_[N/P][3:0] (5)	Input	SerDes receive differential inputs, one differential pair per lane.
SRDS_[3:0]_TX_[N/P][3:0] (4)	Output	SerDes differential Transmit outputs, one differential pair per lane.
Ethernet(19)		
SRDS_45_ATEST (13)	Output	High-impedance output pin probes/forces internal analog nodes during system bring-up.
SRDS_[5:4]_REFCLK_[N/P] (6) (12)	Input	SerDes reference clock supplied from either single-ended or differential external source. Single differential pair per quad.
SRDS_[5:4]_RX_[N/P][3:0] (5)	Input	Receive differential inputs to the SerDes. One differential pair per lane.
SRDS_[5:4]_TX_[N/P][3:0] (4)	Output	SerDes transmit differential outputs. One differential pair per lane.
Miscellaneous		
TS_AN_IO_[1:0]	Input/ Output	Analog I/O pins for test access and calibration. For internal temperature calibration purposes only. Leave unconnected.
DDR4/5 (9, 7, 20)		
DDR45_0_A0_CA_B1	Output	Command/Address (CA) signals Channel B
DDR45_0_A1_PAR_A	Output	Command/Address (CA) signals Channel B (CA_B0 on RDIMM and CA_B13 on UDIMM/component)
DDR45_0_A2_NUL	Output	Command/Address (CA) signals Channel A

Pin Name	Type	Description and Connection Guidelines
DDR45_0_A3_CA_A5	Output	Command/Address (CA) signals Channel A (CA_A5 on RDIMM and CA_A10 on UDIMM/component)
DDR45_0_A4_NULL	Output	Command/Address (CA) signals
DDR45_0_A5_CA_A6	Output	Command/Address (CA) signals Channel A (CA_A6 on RDIMM and CA_A9 on UDIMM/component)
DDR45_0_A6_NULL	Output	Command/Address (CA) signals Channel A
DDR45_0_A7_NULL	Output	Command/Address (CA) signals Channel A
DDR45_0_A8_CA_A4	Output	Command/Address (CA) signals Channel A (CA_A4 on RDIMM and CA_A7 on UDIMM/component)
DDR45_0_A9_CA_A1	Output	Command/Address (CA) signals Channel A (CA_A1 on RDIMM and CA_A3 on UDIMM/component)
DDR45_0_A10_NULL	Output	Command/Address (CA) signals Channel B
DDR45_0_A11_CA_A3	Output	Command/Address (CA) signals Channel A (CA_A3 on RDIMM and CA_A5 on UDIMM/component)
DDR45_0_A12_NULL	Output	Command/Address (CA) signals Channel A
DDR45_0_A13_NULL	Output	Command/Address (CA) signals Channel B
DDR45_0_A17_RSPN_A1	Output	Command/Address (CA) signals (RSPN_A1 on RDIMM and CA_B3 on UDIMM/component)
DDR45_0_ACT_N_NULL	Output	Command/Address (CA) signals Channel A
DDR45_0_BA0_CA_B2	Output	Command/Address (CA) signals (CA_B2 on RDIMM and CA_B11 on UDIMM/component)
DDR45_0_BA1_NULL	Output	Command/Address (CA) signals Channel A
DDR45_0_BG0_CA_A0	Output	Command/Address (CA) signals Channel A
DDR45_0_BG1_CA_A2	Output	Command/Address (CA) signals Channel A (CA_A2 on RDIMM and CA_A1 on UDIMM/component)
DDR45_0_BP_DIGITAL_TESTING	Bidir	Used for digital testing
DDR45_0_BP_MEMRESET_L	Output	SDRAM reset pin controlled by PHY
DDR45_0_BP_VREF_ANALOG_TESTING	Bidir	Used for analog testing
DDR45_0_C0_CA_B4	Output	Command/Address (CA) signals Channel B (CA_B4 on RDIMM and CA_B6 on UDIMM/component)
DDR45_0_C1_RSPN_A0	Output	Command/Address (CA) signals Channel B (RSPN_A0 on RDIMM and CA_B5 on UDIMM/component)
DDR45_0_C2_CA_B6	Output	Command/Address (CA) signals Channel B (CA_B6 on RDIMM and CA_B4 on UDIMM/component)

Pin Name	Type	Description and Connection Guidelines
DDR45_0_CAS_N_NULL	Output	Command/Address (CA) signals Channel B
DDR45_0_CKE0_CSA0	Output	Chip Selects Channel A
DDR45_0_CKE1_CSA1	Output	
DDR45_0_CKE2_CSA2	Output	
DDR45_0_CKE3_CSA3	Output	
DDR45_0_CLK0_C_CK_A0_C	Output	Differential clocks
DDR45_0_CLK0_T_CK_A0_T	Output	
DDR45_0_CLK1_C_NULL	Output	
DDR45_0_CLK1_T_NULL	Output	
DDR45_0_CLK2_C_CK_B0_C	Output	
DDR45_0_CLK2_T_CK_B0_T	Output	
DDR45_0_CLK3_C_NULL	Output	
DDR45_0_CLK3_T_NULL	Output	
DDR45_0_CS_N0_CA_B5	Output	Command/Address (CA) signals Channel B (CA_B5 on RDIMM and CA_B2 on UDIMM/component)
DDR45_0_CS_N1_RSPN_B0	Output	Command/Address (CA) signals Channel B (RSPN_B1 on RDIMM and CA_B0 on UDIMM/component)
DDR45_0_CS_N3_RSPN_B1	Output	Command/Address (CA) signals Channel B
DDR45_0_DM_DBI_UDQS_T_[0:9]	Bidir	SDRAM differential strobes, used for ×4/x16 mode
DDR45_0_DQ_[0:9]_[0:7]	Bidir	SDRAM bidirectional data bus on lanes 0 to 9, bits 0 to 7
DDR45_0_LDQS_C_[0:9]	Bidir	SDRAM differential strobes, used for ×8 mode.

Pin Name	Type	Description and Connection Guidelines
DDR45_0_LDQS_T_[0:9]	Bidir	SDRAM differential strobes, used for ×8 mode.
DDR45_0_MALERT_N_MALERT_N	Output	MALERT
DDR45_0_ODT0_CSB0	Output	Chip Selects Channel B
DDR45_0_ODT0_CSB1	Output	
DDR45_0_ODT0_CSB2	Output	
DDR45_0_ODT0_CSB3	Output	
DDR45_0_PAR_CA_B0	Output	Command/Address (CA) signals Channel A (PAR_A on RDIMM and CA_A12 on UDIMM/component)
DDR45_0_RAS_N_NULL	Output	Command/Address (CA) signals Channel B
DDR45_0_UDQS_C_[0:9]	Bidir	SDRAM differential strobes, used for ×4/x16 mode.
DDR45_0_WE_N_CA_B3	Bidir	Command/Address (CA) signals (CA_B3 on RDIMM and CA_B8 on UDIMM/component)
GDDR6[21]		
GDDR6_[2:0]_C[1:0]_SD_CABI_N [8]	Output	GDDR6 memory active-low command address bus inversion input.
GDDR6_[2:0]_C[1:0]_SD_CA_[9:0] [8]	Output	GDDR6 memory command address inputs.
GDDR6_[3:0]_C[1:0]_SD_CKE_N [8]	Output	GDDR6 memory active-low clock enable input.
GDDR6_[2:0]_C[1:0]_SD_DBI_N_[1:0] [8]	Input/ Output	GDDR6 memory active-low data bus inversion inputs.
GDDR6_[2:0]_C[1:0]_SD_DQ_[15:0] [8]	Input/ Output	Bidirectional data input/output.
GDDR6_[2:0]_C[1:0]_SD_EDC_[1:0] [8]	Input	GDDR6 memory error detection code.
GDDR6_[2:0]_C[1:0]_SD_WCK_[N/P]_[1:0] [8]	Output	Memory differential data clock inputs.
GDDR6_[2:0]_RREF	Input	ZQ calibration reference resistor. Nominal 240Ω resistance to ground, ±1% tolerance.
GDDR6_[2:0]_SD_CLK_[N/P] [8]	Output	Differential memory clock inputs.

Pin Name	Type	Description and Connection Guidelines
GDDR6_[2:0]_SD_RESET_N (8)	Output	GDDR6 memory active-low reset.
GDDR6_1_ATESTCA (13)	Input	CA signals analog voltage monitor.
GDDR6_1_ATESTDQL (13)	Input	Lower DQ signals analog voltage monitor.
GDDR6_1_ATESTDQR (13)	Input	Higher DQ signals analog voltage monitor.

Pin Name	Type	Description and Connection Guidelines

Table Notes

1. Unused I/O can be left unconnected.
2. Do not leave specified pin(s) unconnected.
3. Connect directly to the configuration controller.
4. These pins should be AC coupled. Leave all unused transmit pins unconnected.
5. Leave all unused receive pins unconnected.
6. Connect individual reference clocks for all SerDes quads used in the interface. Optionally, forward a reference clock for one quad to the neighboring quads by selecting **Enable PMA Ref Clock Sharing** in the SerDes IP configuration editor. Tie the unused quads reference clocks to their own individual GND via an optional 50Ω ±1% termination resistor.
7. Connect to the appropriate signals on the DDR device.
8. Connect to the appropriate GDDR6 memory signals. If, the GDDR interface is not used, the I/Os can be left floating.
9. If the DDR interface is not used, the DDR PHY can be set in bypass mode where the unused DDR I/O can be used as special-purpose I/O for low-speed applications such as boundary scan, DC I/O parametric testing, SoC-level ATPG I/O and DDR memory connectivity testing. The direction of these pins is retained from that of the DDR interface. All DDR I/O pins may either be used as special-purpose I/O or the entire set may be used for DDR interfacing, but a combination of both is not allowed. If DDR pins are not used at all, they can be left floating.
10. The JTAG interface pins should be brought out to a JTAG header on the board (the connections must adhere to the JTAG interface standard). These JTAG pins should never be left unconnected and should be connected to a JTAG header even when not used.
11. Requires an off-chip ±1% precision 240Ω resistor terminated to ground.
12. Unused clocks should be tied to their own individual GND via an optional 50Ω ±1% precision termination resistor.
13. Connect directly to observation point.
14. This output is an open-drain signal. In the default mode of operation, it is recommended that this signal be connected to an LED as an indicator on the board.
15. More details about the clock I/O interface can be found in the *Speedster7t Clock and Reset Architecture User Guide* (UG083)[8].
16. More details about the JTAG and configuration interface can be found in the *Speedster7t Configuration User Guide* (UG094)[9].
17. More details about the GPIO interface can be found in the *Speedster7t GPIO User Guide* (UG112)[10].
18. More details about the serdes interface can be found in the *Speedster7t SerDes User Guide* (UG099)[11].
19. More details about the ethernet interface can be found in the *Speedster7t Ethernet User Guide* (UG097)[12].
20. More details about the DDR interface can be found in the *Speedster7t DDR User Guide* (UG096)[13].
21. More details about the GDDR6 interface can be found in the *Speedster7t GDDR6 User Guide* (UG091)[14].

8 https://www.achronix.com/documentation/speedster7t-clock-and-reset-architecture-user-guide-ug083
9 https://www.achronix.com/documentation/speedster7t-configuration-user-guide-ug094
10 https://www.achronix.com/documentation/speedster7t-gpio-user-guide-ug112
11 https://www.achronix.com/documentation/speedster7t-serdes-user-guide-ug099
12 https://www.achronix.com/documentation/speedster7t-ethernet-user-guide-ug097
13 https://www.achronix.com/documentation/speedster7t-ddr-user-guide-ug096
14 https://www.achronix.com/documentation/speedster7t-gddr6-user-guide-ug091

Chapter 3 : Supporting Tables

The following table shows the FCU configuration clock selection based on FCU_CONFIG_SYSCLK_BYPASS, FCU_CONFIG_CLKSEL, and FCU_CONFIG_MODESEL pin selections.

Table 3 • FCU Configuration Clock Selection

FCU_CONFIG_SYSCLK_BYPASS	FCU_CONFIG_CLKSEL	FCU_CONFIG_MODESEL[3:0]	Configuration Clock
0	0	0000, 0001, 0010, 1000 to 1101	On-chip oscillator
1	0	0000, 0001, 0010, 1000 to 1101	CPU clock
X	0	0011, 01XX	CPU clock
X	1	XXXX	JTAG TCK

The following table lists the various error messages that can appear on the error output pins during bitstream programming.

Table 4 • Bitstream Programming Error Output Pins Messages

FCU_CONFIG_ERR_ENC[2:0]	Status	Priority
010	CRC Error.	0 (Lowest)
001	Single-bit/multiple-bit scrubbing error.	1
011	Secure Boot Failure OR Security error.	2
100	Efuse PUF enrollment error.	3
101	Asserted when the AXI interface of the IP configuration space register block does not receive a ready from the master.	4
110	Secure boot authorization error.	5 (Highest)
Other	Undefined.	–

Table 5 • MODESEL Pins FCU Mode Selection

Configuration Mode	FCU_CONFIG_MODESEL[3:0]
CPU x1	0011
CPU x8	0100
CPU x16	0101
CPU x32	0110
CPU x128	0111
Flash SPI (x1)-1D	0001
Flash SPI (x1)-4D	0010
Flash Quad (x2)-1D	1000
Flash Quad (x2)-4D	1010
Flash Quad (x4)-4D	1011
Flash Octa (x8)-1D	1100
Flash Octa (x8)-4D	1101
JTAG	Always active mode

Table 6 • FCU_STATUS Bits Indicating FCU State

FCU_STATUS	State
11	fcu_locked.
10	sync_found.
01	ID found.
00	Instance ID found/FCU unlocked.

Chapter 4 : Power Pin Connections

Please refer to the **Speedster7t Power User Guide (UG087)**[15] for a detailed description of the power and ground pins on Speedster7t devices.

15 https://www.achronix.com/documentation/speedster7t-power-user-guide-ug087

Chapter 5 : Revision History

Version	Date	Description
1.0	24 May 2019	• Initial Achronix release
1.1	11 Jun 2019	• Removed double prefixes from FCU, JTAG and TS pin names • Renamed UDQS_T signals in DDR4 interface to DM_DBI_UDQS_T and DM_DBI_UDQS_C signals to UDQS_C • Updated FCU Io pins to include strap signals, stap_sel and error status signals • Updated GDDR6 ATEST signals for the East and West sides
1.2	21 Apr 2020	• Reverted some of the clock or High-Z signals to be input or output • Updated connection guidelines for a few FCU_* pins • Updates to the to the CLKIO_* pin description to include additional supported standards and use-cases • Corrections to the FCU_CONFIG_ERR_ENC[2:0] bit status to match hardware • Updated DDR I/O in bypass mode use cases
1.3	08 May 2020	• Complete restructuring of the user guide for better readability • Updated connection guidelines for DDR4 I/O in bypass mode
1.4	08 May 2021	• Minor edits and corrections
1.5	29 Sep 2021	• Updated recommended pull-up/pull-down resistor values for FCU pins • Updated open-drain specification for FCU pins • Updated FCU Mode Selection and FCU Error Status tables
1.6	25 Apr 2022	• Clarify usage of MSIO/REFIO pins as reset inputs to IP subsystems or core
>1.7	30 Jan 2024	• Updated recommended pull-up and pull down impedance values for the FCU pins based on the Speedster7t1500 A1 silicon.
1.8	04 Dec 2024	▪ Added information on AC7t800
1.9	08 Oct 2026	• Added information on AC7t700 • Clarify FCU_CONFIG_DONE and FCU_PARTIAL_CONFIG_DONE usage