
Speedster7t Pin Connectivity User Guide (UG084)

Speedster FPGAs

Preliminary Data



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Preliminary Data

This document contains preliminary information and is subject to change without notice. Information provided herein is based on internal engineering specifications and/or initial characterization data.

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Chapter - 1: Introduction

This user guide lists each of the I/O pin groups available in the Speedster7t 7t1500 device, their functionality and recommended connection guidelines. Refer to the *Speedster7t Power User Guide* (UG087) for detailed description on the power/ground pins.

Chapter - 2: Pin List and Connection Guidelines

Pin Name	Type	Description and Connection Guidelines
Clock I/O Interface		
CLKIO_NE_MSIO_[N/P]	Input /Output	A group of two clock buffers in each corner of the device that can be used either as a single pseudo-differential clock I/O or two single-ended clock I/O. The supported voltage levels are 1.5V and 1.8V. If these I/O are not used as clock buffers, they can be used only as reset inputs. ⁽¹⁾
CLKIO_NW_MSIO_[N/P]		
CLKIO_SE_MSIO_[N/P]		
CLKIO_SW_MSIO_[N/P]		
CLKIO_NE_MSIO_ZCAL	Input	Impedance calibration inputs, one for each CLKIO bank, common for both on-die termination and output driver. ⁽¹¹⁾
CLKIO_NW_MSIO_ZCAL		
CLKIO_SE_MSIO_ZCAL		
CLKIO_SW_MSIO_ZCAL		
CLKIO_NE_REFIO_[N/P]_0	Input /Output	A set of eight differential reference clock input/output pairs, two in each corner of the device. ⁽¹⁾ If these I/O are not used as clock buffers, each REFIO pair can receive up to two reset inputs. The REFIO supports the following configurations: <ul style="list-style-type: none"> • LVDS and LVPECL input signals up to a frequency of 1GHz. The LVPECL I/O also requires board-level AC coupling capacitors. • LVDS test output capability. • LVCMOS input/output at 1.5V and 1.8V
CLKIO_NE_REFIO_[N/P]_1		
CLKIO_NW_REFIO_[N/P]_0		
CLKIO_NW_REFIO_[N/P]_1		
CLKIO_SE_REFIO_[N/P]_0		
CLKIO_SE_REFIO_[N/P]_1		
CLKIO_SW_REFIO_[N/P]_0		
CLKIO_SW_REFIO_[N/P]_1		
CLKIO_NE_VREF	Input	Optional external reference voltage supply to the CLKIO, typically set to CLKIO*_VDDIO/2 when supplied externally. When this voltage is internally supplied by the MSIO macro, these pins should be connected to ground.
CLKIO_NW_VREF		
CLKIO_SE_VREF		
CLKIO_SW_VREF		
IEEE1149.1/1149.6 JTAG Interface⁽¹⁰⁾		

Pin Name	Type	Description and Connection Guidelines
JTAG_TCK	Input	Dedicated test clock used to advance the TAP controller and clock in data on the TDI input and out on the TDO output. The maximum frequency for TCK is 25 MHz.
JTAG_TDI	Input	Serial input for instruction and test data. Data is captured on the rising edge of the test logic clock (TCK).
JTAG_TDO	Output	Serial output for data from the test logic. TDO is set to an inactive drive state (high impedance) when data scanning is not in progress. TDO drives out valid data on the falling edge of the TCK input.
JTAG_TMS	Input	Test mode select (TMS) input controlling the test access port (TAP) controller state machine transitions. This input is captured on the rising edge of the test logic clock (TCK).
JTAG_TRSTN	Input	Active-low reset input used to initialize the TAP controller
Configuration Interface		
FCU_CONFIG_BYPASS_CLEAR	Input	Active-high input pin to bypass configuration memory clear during device initialization. This input should be tied to GND if it is not used. ⁽²⁾
FCU_CONFIG_CLKSEL	Input	Pin controlling whether the FPGA configuration unit (FCU) clock is sourced from the TCK input or the CPU_CLK input (see Table: FCU Configuration Clock Selection Based). (see page 15) It should be connected to a configurable input such as a DIP switch to toggle between modes of operation for debug. If this is not possible or desired, tie this signal off to 1.8V (FCU_CB_VDDIO) or GND based on the desired clock for the configuration mode. ⁽²⁾
FCU_CONFIG_ERR_ENC[2:0]	Output	Active-high output pins highlighting the presence of a CRC, scrubbing or other errors in the bitstream during device programming. If asserted, it continues to stay high, and users should expect that configuration loading never completes, and user mode is never entered (see Table: Error Output Pins). (see page 15) Connect these pins directly to error indicator.
FCU_CONFIG_DONE	Output (14)	Active-high configuration done output signal indicating that bitstream loading completed successfully and that the device is ready to enter user mode. When high, the signal remains asserted until the FCU is power cycled or reset for a re-initialization sequence. If a device configuration error occurs, the CONFIG_DONE output remains low. Holding this pin low on the board can be used to synchronize the start-up of multiple devices.

Pin Name	Type	Description and Connection Guidelines
FCU_CONFIG_MODESEL_[3:0]	Input	Configuration mode selection inputs to define the FCU mode of operation (see Table: FCU Mode Selection). (see page 15) These inputs should be connected to configurable inputs, such as DIP switches, to toggle between modes of operation for debug. If this is not possible or desired based on the config scheme, these pins should be tied to FCU_CB_VDDIO or GND. ⁽²⁾
FCU_PARTIAL_CONFIG_DONE	Output	Active-high, open-drain configuration done output signal indicating that bitstream loading completed successfully for partial reconfiguration of the device, and that the device is ready to enter user mode. Connect this output directly to an indicator LED or configuration controller.
FCU_CONFIG_RSTN	Input	Asynchronous active-low reset input clearing the configuration memory in the device and the logic in the FCU. ⁽³⁾ Pull-up/pull-down options can be implemented in one of two ways: <ul style="list-style-type: none"> • If the configuration controller is always driving this input, the pin can be pulled down to GND using a 4.7 kΩ ±5% resistor to ensure that the FPGA is in a reset state on power-up. • If the pin is sometimes not driven by the configuration controller or tristated, it is imperative that it be pulled up to 1.8 V (FCU_CB_VDDIO) through a 4.7 kΩ ±5% resistor.
FCU_STRAP_[2:0]	Output	Unconnected spare outputs. Leave these pins unconnected.
FCU_STAP_SEL	Input	When asserted high, this signal enables the JTAG interface pins to be directly connected to the JTAG controller in the SerDes PMA blocks allowing for SerDes configuration, debug and performance monitoring directly from the JTAG interface. For bitstream download and design debug using the JTAG interface, this pin must be held low. For SerDes PMA debug only mode, this pin must be held high. ⁽²⁾ This input must be connected to a configurable input, such as a DIP switch, to toggle between modes of operation for debug. If this pin is not used then it should be tied to GND using a 10 kΩ pull-down resistor
FCU_CONFIG_STATUS	Output (14)	Active-high configuration status output signal indicating that the FCU has completed initial start-up and has cleared the CMEM and is awaiting FCU commands for bitstream programming. When high, the signal remains asserted until the FCU is power cycled, reset for a re-initialization sequence, or a CRC error is seen during bitstream load.
FCU_CONFIG_SYSCLK_BYPASS	Input	Active-high setting to bypass configuration system clock. Along with CFG_CLKSEL, this setting allows for clock selection during programming (see Table: FCU Configuration Clock Selection Based (see page 15)). This input should be connected to a configurable input, such as a DIP switch, to toggle between modes of operation for debug. If this is not possible or desired, tie this off to 1.8V (FCU_CB_VDDIO) or GND based on the desired clock for the configuration mode. ⁽²⁾

Pin Name	Type	Description and Connection Guidelines
FCU_CONFIG_USER_MODE	Output	Active-high output indicating that the device has transitioned into user mode. When high, the signal remains asserted until the FCU is power cycled or reset for a re-initialization sequence. This signal is not an open drain output; therefore, it can be connected directly to an indicator LED or configuration controller.
FCU_CPU_CLK	Input	Input clock from an external CPU. The data/address bus is synchronous to this clock. If the CPU_CLK is not used to source the FCU clock, then this pin should be tied to GND.
FCU_CPU_CSN	Input	Active-low CPU mode chip select. Connect the CSN pin directly to the configuration controller. If this pin is not used, this pin should be pulled high using a pull-up resistor.
FCU_CPU_DQ_IN_OUT[31:0]	Input /Output	Data input/output pins shared between the CPU and flash interfaces. The CPU interface is inaccessible when flash mode is in use and vice-versa. If any pins are unused based on the configuration, then they should be connected to weak pull-up resistors. ⁽³⁾
FCU_CPU_DQ_VALID	Output	Active-high control bit to indicate to the CPU the clock cycles when the CPU_DQ bus has valid read-back data. Synchronous to FCU_CPU_CLK. ⁽³⁾
FCU_LOCK	Output	Active-high status bit to indicate the FCU lock/unlock status. ⁽³⁾
FCU_STATUS_[1:0]	Output	FCU status bits showing the FCU state are shown in Table: FCU_STATUS Bits. (see page 16) ⁽³⁾
FCU_FLASH_CSN_[3:0]	Output	Active-low chip select to enable/disable one or more of the attached flash memory devices: <ul style="list-style-type: none"> For ×1 mode, only CSN[0] is used; leave CSN[3:1] unconnected. For ×4 mode, connect each CSN[3:0] to a flash device. Connect all four to the individual signals to serial flash devices.
FCU_FLASH_HOLDN	Output	Active-low hold output to flash memory device(s). This signal is used to pause serial communications between the FPGA and the flash device without deselecting the device or stopping the serial clock. Synchronous to FLASH_SCK. ⁽³⁾
FCU_FLASH_SCK	Output	Clock output from the FCU to the flash memory device(s). Connect this clock directly to the flash device(s).
FCU_OSC_CLK	Output	This clock is internally generated from a ring oscillator. For debug purposes, it can be bypassed, and the external clock CPU_CLK can be used. ⁽³⁾
General Purpose I/O Interface		

Pin Name	Type	Description and Connection Guidelines
GPIO_[N0/S0]_BYTE[2:0]_VREF	Input	Optional external reference voltage supply to the GPIO. This supply is typically connected to GPIO_VDDIO/2 when supplied externally. When this voltage is supplied internally by the MSIO macro, these pins should be connected to ground.
GPIO_[N0/S0]_ZCAL	Input	Impedance calibration input, one for each GPIO bank, common for both on-die termination and output driver. ⁽¹¹⁾
GPIO_[N0/S0]_BYTE[1:0]_BIT_[11:0]	Input /Output	Single-ended GPIO that support multiple I/O standards at multiple voltages. Bytes 0 and 1 contain a group of 12 I/O out of which ten are dedicated to data and two are dedicated to clock. Byte 2 has a group of 8 I/O out of which six are dedicated to data and two are dedicated to clock. Pseudo-differential pairs can be built using two adjacent buffers. ⁽¹⁾
GPIO_[N0/S0]_BYTE2_BIT_[7:0]		
SerDes		
PCIe_x16		
SRDS_N03_ATEST	Output	High-impedance output pin to probe/force internal analog nodes during system bring-up. ⁽¹³⁾
SRDS_N[3:0]_REFCLK_[N/P]	Input	SerDes reference clock supplied from either a single-ended or differential external source. There is single differential pair for each quad. Each SerDes quad has a common reference clock. For PCIe ×16 mode, the reference clocks for all the SerDes quads need to be connected. ^(6,12)
SRDS_N[3:0]_RX_[N/P][3:0]	Input	Receive differential inputs to the SerDes. There is one differential pair per each lane. ⁽⁵⁾
SRDS_N[3:0]_TX_[N/P][3:0]	Output	Transmit differential outputs from the SerDes. There is one differential pair per each lane. ⁽⁴⁾
Ethernet		
SRDS_N47_ATEST	Output	High-impedance output pin to probe/force internal analog nodes during system bring-up. ⁽¹³⁾
SRDS_N[5:4]_REFCLK_[N/P]	Input	SerDes reference clock supplied from either a single-ended or differential external source. There is a single differential pair for each quad. ^(6,12)
SRDS_N[5:4]_RX_[N/P][3:0]	Input	Receive differential inputs to the SerDes. There is one differential pair per each lane. ⁽⁵⁾
SRDS_N[5:4]_TX_[N/P][3:0]	Output	Transmit differential outputs from the SerDes. There is one differential pair per each lane. ⁽⁴⁾

Pin Name	Type	Description and Connection Guidelines
Shared PCIe_x8 and Ethernet		
SRDS_N[7:6]_REFCLK_[N/P]	Input	SerDes reference clock supplied from either a single-ended or differential external source. There is one differential pair for each quad. ⁽⁶⁾ If the SerDes is configured to be in PCIe-compliant ×8 mode, the reference clocks for all 8 SerDes lanes need to be connected. If SerDes is configured to operate as non-PCIe compliant ×4 mode, the unused lanes' clocks should be tied to their own individual GND via an optional 50Ω ±1% termination resistor.
SRDS_N[7:6]_RX_[N/P][3:0]	Input	Receive differential inputs to the SerDes. There is one differential pair per each lane. ⁽⁵⁾
SRDS_N[7:6]_TX_[N/P][3:0]	Output	Transmit differential outputs from the SerDes. There is one differential pair per each lane. ⁽⁴⁾
Miscellaneous		
TS_AN_IO_[1:0]	Input /Output	Analog I/O pins used for test access and calibration. These pins are used for internal temperature calibration purposes only. Leave unconnected.
DDR4⁽⁹⁾		
DDR4_S0_A17	Output	Address input to the SDRAM (used in the ×4 configuration only). ⁽⁷⁾
DDR4_S0_ACT_N	Output	Active-low ACTIVATE command to the SDRAM. ⁽⁷⁾
DDR4_S0_A_[13:0]	Output	Bank address inputs to the SDRAM. ⁽⁷⁾
DDR4_S0_BA_[1:0]	Output	Bank select Inputs to the SDRAM. ⁽⁷⁾
DDR4_S0_BG_[1:0]	Output	Bank group inputs to the SDRAM. ⁽⁷⁾
DDR4_S0_BP_ALERT_N	Input /Output	I/O signal driven by the DDR4 SDRAM to signal to the host controller when the SDRAM detects an error on the DDR interface, or it is a signal driven by the host controller to the SDRAM during connectivity test mode. ⁽⁷⁾
DDR4_S0_BP_MEMRESET_L	Output	Active-low memory reset signal to external SDRAM. ⁽⁷⁾
DDR4_S0_BP_VREF	Input /Output	Reference voltage to external SDRAM. ⁽⁷⁾
DDR4_S0_BP_ZN	Output	External calibration reference resistor. Supported calibration resistor values are 40Ω, 120Ω and 240Ω ±1%.

Pin Name	Type	Description and Connection Guidelines
DDR4_S0_CAS_N	Output	Active-low column address select signal to external SDRAM. When ACT_N and CS_N are low, these outputs are interpreted as column address bits. When ACT_N is high, these outputs are interpreted as command pins to indicate READ, WRITE or other commands. ⁽⁷⁾
DDR4_S0_CID_[2:0]	Output	Chip ID select for stacked components. ⁽⁷⁾
DDR4_S0_CKE_[3:0]	Output	SDRAM clock enable control signal. ⁽⁷⁾
DDR4_S0_CK_[N/P]_[3:0]	Output	Differential clock inputs to the SDRAM. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_T and the negative edge of CK_C. ⁽⁷⁾
DDR4_S0_CS_N_[3:0]	Output	Active-low chip select signals to external SDRAM. All commands are masked when CS_n is registered high. CS_N provides external rank selection on systems with multiple ranks. ⁽⁷⁾
DDR4_S0_UDQS_N_[8:0]	Input /Output	Data mask and data bus inversion signals to the SDRAM. ⁽⁷⁾
DDR4_S0_DQ_[8:0]_[7:0]	Input /Output	SDRAM data bus. ⁽⁷⁾
DDR4_S0_LDQS_[N/P]_[8:0]	Input /Output	SDRAM data strobe signals. ⁽⁷⁾
DDR4_S0_ODT_[3:0]	Output	SDRAM on-die termination control signal. ODT resistances can be configured to one of these values (open, 240, 120, 80, 60, 48, 40) pulled up to DDR4_S0_VDDQ.
DDR4_S0_PAR	Output	Command/address parity input to the SDRAM. ⁽⁷⁾
DDR4_S0_RAS_N	Output	Active-low row address select signal to external SDRAM. When ACT_N and CS_N are low, these outputs are interpreted as row address bits. When ACT_N is high, these outputs are interpreted as command pins to indicate READ, WRITE or other commands. ⁽⁷⁾
DDR4_S0_DM_DBI_UDQS_P_[8:0]	Input /Output	SDRAM data strobe signals. ⁽⁷⁾
DDR4_S0_WE_N	Output	Active-low write enable signal. ⁽⁷⁾
GDDR6		
GDDR6_[E/W][3:0]_C[1:0]_SD_CABI_N	Output	Active-low command address bus inversion input to the GDDR6 memory. ⁽⁸⁾
GDDR6_[E/W][3:0]_C[1:0]_SD_CA_[9:0]	Output	Command address inputs to the GDDR6 memory. ⁽⁸⁾

Pin Name	Type	Description and Connection Guidelines
GDDR6_[E/W][3:0]_C[1:0]_SD_CKE_N	Output	Active-low clock enable input to the GDDR6 memory. ⁽⁸⁾
GDDR6_[E/W][3:0]_C[1:0]_SD_DBI_N[1:0]	Input /Output	Active-low data bus inversion inputs to the GDDR6 memory. ⁽⁸⁾
GDDR6_[E/W][3:0]_C[1:0]_SD_DQ_[15:0]	Input /Output	Bidirectional data input/output. ⁽⁸⁾
GDDR6_[E/W][3:0]_C[1:0]_SD_EDC_[1:0]	Input	Error detection code from the GDDR6 memory. ⁽⁸⁾
GDDR6_[E/W][3:0]_C[1:0]_SD_WCK_[N/P]_[1:0]	Output	Differential data clock inputs to memory. ⁽⁸⁾
GDDR6_[E/W] [3:0]_RREF	Input	Reference resistor for ZQ calibration. Nominal 240Ω, ±1% tolerance resistance to ground.
GDDR6_[E/W] [3:0]_SD_CLK_[N/P]	Output	Differential clock inputs to the memory. ⁽⁸⁾
GDDR6_[E/W] [3:0]_SD_RESET_N	Output	Active-low reset to the GDDR6 memory. ⁽⁸⁾
GDDR6_E2_ATESTCA	Input	Analog voltage monitor for CA signals. ⁽¹³⁾
GDDR6_E2_ATESTDQL	Input	Analog voltage monitor for the lower DQ signals. ⁽¹³⁾
GDDR6_E2_ATESTDQR	Input	Analog voltage monitor for the higher DQ signals. ⁽¹³⁾
GDDR6_W1_ATESTCA	Input	Analog voltage monitor for CA signals. ⁽¹³⁾
GDDR6_W 1_ATESTDQL	Input	Analog voltage monitor for the lower DQ signals. ⁽¹³⁾
GDDR6_W 1_ATESTDQR	Input	Analog voltage monitor for CA signals. ⁽¹³⁾

Pin Name	Type	Description and Connection Guidelines
<p>Table Notes</p> <ol style="list-style-type: none"> 1. Unused I/O can be left unconnected. 2. Do not leave this/these pin(s) unconnected. 3. Connect directly to the configuration controller. 4. These pins should be AC coupled. Leave all unused transmit pins unconnected. 5. Leave all unused receive pins unconnected. 6. Connect these clocks for all SerDes lanes used in the interface. 7. Connect to the appropriate signals on the DDR4 DIMM. 8. Connect to the appropriate GDDR6 memory signals. 9. If the DDR4 interface is not used, the DDR PHY can be set in bypass mode where the unused DDR4 I/O can be used as special-purpose I/O for low-speed applications such as boundary scan, DC I/O parametric testing, SoC-level ATPG I/O and DDR4 memory connectivity testing. The direction of these pins is retained from that of the DDR4 interface. The user can either use all DDR I/O as special-purpose I/O or use the entire set for DDR4 interfacing, but a combination of both is not allowed. 10. The JTAG interface pins should be brought out to a JTAG header on the board, and the connections must adhere to the JTAG interface standard. These JTAG pins should never be left unconnected and should be connected to a JTAG header even when not used. 11. Requires an off-chip $\pm 1\%$ precision 240Ω resistor terminated to ground. 12. Unused clocks should be tied to their own individual GND via an optional $\pm 1\%$ precision 50Ω termination resistor. 13. Connect directly to observation point. 14. This output is an open-drain signal. In the default mode of operation, it is recommended that this signal be connected to an LED as an indicator on the board. In this case, use an external $10\text{ k}\Omega \pm 5\%$ pull-up resistor to 3.3V and drive a $1\text{ k}\Omega$ resistor to the input of a FET to turn on the LED. If LED usage is not desired, this signal must be pulled-up to 1.8V (FCU_CB_VDDIO) instead using the same $10\text{ k}\Omega$ pull-up resistor. 		

Chapter - 3: Supporting Tables

Table 1: FCU Configuration Clock Selection Based on SYSCLK_BYPASS and CLKSEL Pin Selections

SYSCLK_BYPASS	CFG_CLKSEL	CFG_MODESEL[3:0]	Configuration Clock
0	0	0000, 0001, 0010, 1000 to 1101	On-chip oscillator
1	0	0000, 0001, 0010, 1000 to 1101	CPU clock
X	0	0011, 01XX	CPU clock
X	1	XXXX	JTAG TCK

Table 2: Error Output Pins Indicating Various Error Messages During Bitstream Programming

FCU_CONFIG_ERR_ENC [2:0]	Status	Priority
001	CRC error.	0 (Lowest)
010	Single-bit/multiple-bit scrubbing error.	1
011	Secure boot failure or a security error.	2
100	Efuse PUF enrollment error.	3
101	Asserted when AXI interface of the IP configuration space register block does not receive a ready from the master.	4 (Highest)
Other	Undefined.	

Table 3: FCU Mode Selection Based on MODESEL Pins

Configuration Mode	CFG_MODESEL[3:0]
Flash Serial ×1	0001
Flash Serial ×4	0010
CPU ×1, ×8, ×16, ×32, ×128	0011 to 0111
Flash Dual ×1	1000
Flash Dual ×4	1001

Configuration Mode	CFG_MODESEL[3:0]
Flash Quad ×1	1010
Flash Quad ×4	1011
Flash Octa ×1	1100
Flash Octa ×4	1101
JTAG	Always active mode

Table 4: FCU_STATUS Bits Indicating FCU State

FCU_STATUS	State
11	fcu_locked
10	sync_found
01	ID found
00	instance ID found / FCU unlocked

Chapter - 4: Revision History

Version	Date	Description
1.0	24 May 2019	<ul style="list-style-type: none"> Initial Achronix release.
1.1	11 Jun 2019	<ul style="list-style-type: none"> Removed double prefixes from FCU, JTAG and TS pin names. Renamed UDQS_T signals in DDR4 interface to DM_DBI_UDQS_T and DM_DBI_UDQS_C signals to UDQS_C. Updated FCU I/O pins to include strap signals, stap_sel and error status signals Updated GDDR6 ATEST signals for the East and West sides.
1.2	21 Apr 2020	<ul style="list-style-type: none"> Reverted some of the clock or High-Z signals to be input or output. Updated connection guidelines for a few FCU_* pins. Updates to the CLKIO_* pin description to include additional supported standards and use-cases. Corrections to the FCU_CONFIG_ERR_ENC[2:0] bit status to match hardware. Updated DDR I/O in bypass mode use cases
1.3	08 May 2020	<ul style="list-style-type: none"> Complete restructuring of the user guide for better readability. Updated connection guidelines for DDR4 I/O in bypass mode.
1.4	08 May 2021	<ul style="list-style-type: none"> Minor edits and corrections.