Speedster7t Pin Connectivity User Guide (UG084)

For Speedster7t Devices

Achronix®

Data Acceleration

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Chapter - 1: Introduction

This user guide lists each of the I/O pin groups available in the Speedster7t 7t1500 device, their functionality and recommended connection guidelines. Refer to the Power User Guide for detailed description on the power/gnd pins

Chapter - 2: Pin List and Connection Guidelines

Pin Name	Pin Group	Type	Description	Connection Guidelines
Clock I/O Interface				
CLKIO_NE_MSIO_[N/P]	CLK	Input /Output	A group of two clock buffers in each corner of the device that can be used either as a single differential clock I/Os or two single-ended clock I/Os. If these I /Os are not used as clock buffers, they can be used as generic inputs or outputs	Unused I/O can be left unconnected.
CLKIO_NW_MSIO_[N/P]				
CLKIO_SE_MSIO_[N/P]				
CLKIO_SW_MSIO_[N/P]				
CLKIO_NE_MSIO_ZCAL	CLK	Input	Impedance calibration input, one for each CLKIO bank.	Requires an off-chip precision resistor 240Ω ±1% terminated to ground.
CLKIO_NW_MSIO_ZCAL				
CLKIO_SE_MSIO_ZCAL				
CLKIO_SW_MSIO_ZCAL				
CLKIO_NE_REFIO_[N/P]_0	CLK	Input /Output	A set of eight differential reference clock Input/Output pairs, two in each corner of the device. REFIO can support LVDS and LVPECL input signals up to a frequency of 1GHz. Additionally, the REFIO supports LVDS test output capability.	Unused I/Os can be left unconnected.
CLKIO_NE_REFIO_[N/P]_1				
CLKIO_NW_REFIO_[N/P]_0				
CLKIO_NW_REFIO_[N/P]_1				
CLKIO_SE_REFIO_[N/P]_0				
CLKIO_SE_REFIO_[N/P]_1				

Pin Name	Pin Group	Type	Description	Connection Guidelines
CLKIO_SW_REFIO_[N/P]_0				
CLKIO_SW_REFIO_[N/P]_1				
CLKIO_NE_VREF	CLK	Input	External reference voltage supply to the GPIO	Typically set to CLKIO_*_VDDIO/2.
CLKIO_NW_VREF				
CLKIO_SE_VREF				
CLKIO_SW_VREF				
IEEE1149.1/1149.6 JTAG Interface				**Do not leave JTAG I/Os unconnected. The JTAG interface should be brought out to a JTAG header on the board**
JTAG_TCK	JTAG	Input	Dedicated test clock used to advance the TAP controller and clock in data on TDI input and out on TDO output. The maximum frequency for TCK is 50MHz.	Connect this pin using a 1-kΩ ±1% pull-down resistor to GND.
JTAG_TDI	JTAG	Input	Serial input for instruction and test data. Data is captured on the rising edge of the test logic clock.	Connect this pin using a 10-kΩ ±5% pull-up resistor to FCU_CB_VDDIO (1.8V).
JTAG_TDO	JTAG	Output	Serial output for data from the test logic. TDO is set to an inactive drive state (high impedance) when data scanning is not in progress. TDO drives out valid data on the falling edge of the TCK input.	Connect this pin using a 10-kΩ ±5% pull-up resistor to FCU_CB_VDDIO (1.8V) to minimize leakage in the TDI input buffer of interfacing devices.
JTAG_TMS	JTAG	Input	Test Mode Select (TMS) input controlling the test access port (TAP) controller state machine transitions. This input is captured on the rising edge of the test logic clock (TCK).	Connect this pin using a 10-kΩ ±5% pull-up resistor to FCU_CB_VDDIO (1.8V).
JTAG_TRSTN	JTAG	Input	Active-low reset input used to initialize the TAP controller	Connect this pin using a 4.7- kΩ ±5% pull-down resistor to GND.
Configuration Interface				

<table>
<tr><th>Pin Name</th><th>Pin Group</th><th>Type</th><th>Description</th><th>Connection Guidelines</th></tr>
<tr><td>FCU_CFG_BYPASS_CLEAR</td><td>CFG</td><td>Input</td><td>Active-high input pin to bypass configuration memory clear during device initialization.</td><td>Do not leave this pin unconnected. It should be tied to GND.</td></tr>
<tr><td>FCU_CFG_CLKSEL</td><td>CFG</td><td>Input</td><td>Pin controlling whether the FCU clock is sourced from the TCK input or the CPU_CLK input.
<table>
<tr><th>SYSCLK_BYPASS</th><th>CFG_CLKSEL</th><th>CFG_MODESEL[3:0]</th><th>Configuration Clock</th></tr>
<tr><td>0</td><td>0</td><td>0000, 0001, 0010 1000 to 1101</td><td>On-chip Oscillator</td></tr>
<tr><td>1</td><td>0</td><td>0000, 0001, 0010,1000 to 1101</td><td>CPU clock</td></tr>
<tr><td>X</td><td>0</td><td>0011, 01XX</td><td>CPU clock</td></tr>
<tr><td>X</td><td>1</td><td>XXXX</td><td>JTAG TCK</td></tr>
</table></td><td>Do not leave this pin unconnected. It should be connected to a configurable input like a DIP switch to toggle between modes of operation for debug. If this is not possible or desired, tie this off to 1.8V (FCU_CB_VDDIO) or GND based on the desired clock for the configuration mode.</td></tr>
<tr><td>FCU_CFG_ERR_ENC[2:0]</td><td>CFG</td><td>Output</td><td>Active-high output pins highlighting the presence of a CRC,scrubbing or other errors in the bitstream during device programming. If asserted, it continues to stay high and users should expect that configuration loading never complete, and user mode is never entered.</td><td>Connect these pins directly to error indicator.</td></tr>
<tr><td>FCU_CFG_DONE</td><td>CFG</td><td>Output</td><td>Active-high configuration done output signal indicating that bitstream loading completed successfully and that the device is ready to enter user mode. Once high, it stays asserted until the FCU is power cycled or reset for a re-initialization sequence.If a device configuration error occurs, the CONFIG_DONE output will remain low. Holding this pin low on the board can be used as a method to synchronize the start-up of multiple devices.</td><td>In the default mode of operation, it is recommended that this signal be connected to an LED as an indicator on the board. In this case, use an external 10-kΩ ±5% pull-up resistor to 3.3 V and drive a 1-kΩ resistor to the input of a FET to turn on the LED. If LED usage is not desired, this signal can be pulled-up to 1.8V (FCU_CB_VDDIO) instead using the same 10-kΩ pull-up resistor</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>Pin Group</th><th>Type</th><th>Description</th><th>Connection Guidelines</th></tr>
<tr><td>FCU_CFG_MODESEL_[3:0]</td><td>CFG</td><td>Input</td><td>Configuration mode selection inputs to define the FPGA configuration unit (FCU) mode of operation.
<table>
<tr><th>Configuration Mode</th><th>CFG_MODESEL[3:0]</th></tr>
<tr><td>Flash Serial 1x</td><td>0001</td></tr>
<tr><td>Flash Serial 4x</td><td>0010</td></tr>
<tr><td>CPU x1,x8,x16,x32,x128</td><td>0011 to 0111</td></tr>
<tr><td>Flash Dual x1</td><td>1000</td></tr>
<tr><td>Flash Dual x4</td><td>1001</td></tr>
<tr><td>Flash Quad x1</td><td>1010</td></tr>
<tr><td>Flash Quad x4</td><td>1011</td></tr>
<tr><td>Flash Octa x1</td><td>1100</td></tr>
<tr><td>Flash Octa x4</td><td>1101</td></tr>
<tr><td>JTAG</td><td>Always active mode</td></tr>
</table></td><td>Do not leave these pins unconnected. They should be connected to configurable inputs like DIP switches to toggle between modes of operation for debug. If this is not possible or desired, based on the config scheme, these pins should be tied to FCU_CB_VDDIO or GND.</td></tr>
<tr><td>FCU_CFG_PARTIAL_RECONFIG_DONE</td><td>CFG</td><td>Output</td><td>Active-high configuration done output signal indicating that bitstream loading completed successfully for partial reconfiguration of the device and that the device is ready to enter user mode.</td><td>Connect this pin directly to an indicator or configuration controller</td></tr>
</table>

Pin Name	Pin Group	Type	Description	Connection Guidelines
FCU_CFG_RSTN	CFG	Input	Asynchronous active-low reset input clearing the configuration memory in the device and the logic in the FPGA configuration unit (FCU).	Connect directly to the configuration controller. Pull-up/pull-down options can be done in one of two ways: • If the configuration controller will always be driving this input, the pin can be pulleddown to GND using a 4.7-kΩ ±5% resistor to ensure that the FPGA will be in a reset state on power-up. • If the pin may sometimes not be driven by the configuration controller or tristated, it Is imperative that it be pulled-up to 1.8V (FCU_CB_VDDIO) through a 4.7-kΩ ±5% resistor
FCU_STRAP_[2:0]	CFG	High-Z	Unconnected spare outputs	Leave these pins unconnected
FCU_STAP_SEL	CFG	Input	When asserted high, this signal enables the JTAG interface pins to be directly connected to the JTAG controller in the SerDes PMA blocks allowing SerDes configuration, debug and performance monitoring directly from the JTAG interface. For bitstream download and design debug using the JTAG interface, this pin must be held low. For SerDes PMA debug only mode, this pin must be held high.	Do not leave this pin unconnected. It must be connected to a configurable input such as a DIP switch to toggle between modes of operation for debug.
FCU_CFG_STATUS	CFG	Output	Active-high configuration status output signal indicating that the FCU has completed initial start-up and has cleared the CMEM and is awaiting FCU commands for bitstream programming. Once high, it stays asserted until the FCU is power cycled or reset for a re-initialization sequence or a CRC error is seen during bitstream load.	It is recommended to connect this signal to an LED as an indicator on the board. In this case, use an external 10-kΩ ±5% pull-up resistor to 3.0V/3.3V and drive a 1-kΩ resistor to the input of a FET to turn on the LED. If LED usage is not desired, this signal can be pulled-up to 1.8V (FCU_CB_VDDIO) using the same 10-kΩ pull-up resistor.
FCU_CFG_SYSCLK_BYPASS	CFG	Input	Active-high bypass configuration system clock setting. Along with CFG_CLKSEL, this setting allows for clock selection during programming.	Do not leave this pin unconnected. It should be connected to a configurable input like a DIP switch to toggle between modes of operation for debug. If this is not possible or desired, tie this off to 1.8V (FCU_CB_VDDIO) or GND based on the desired clock for the configuration mode.
FCU_CFG_USER_MODE	CFG	Output	Active-high output indicating that the device has transitioned into user mode. Once high, it stays asserted until the FCU is power cycled or reset for a re-initialization sequence.	Connect directly to an indicator or configuration controller

<table>
<tr><th>Pin Name</th><th>Pin Group</th><th>Type</th><th>Description</th><th>Connection Guidelines</th></tr>
<tr><td>FCU_CPU_CLK</td><td>CFG</td><td>clock</td><td>Input clock from external CPU. The data/address bus is synchronous to this clock.</td><td>If the CPU_CLK is not used to source the FCU clock, then pin should be tied to GND.</td></tr>
<tr><td>FCU_CPU_CSN</td><td>CFG</td><td>Input</td><td>Active-low CPU mode chip select.</td><td>Connect the CSN pin directly to the configuration controller.</td></tr>
<tr><td>FCU_CPU_DQ_[31:0]</td><td>CFG</td><td>Input /Output</td><td>Input pins providing data input to and from the CPU</td><td>Connect directly to the configuration controller.</td></tr>
<tr><td>FCU_CPU_DQ_VALID</td><td>CFG</td><td>Output</td><td>Active-high control bit to indicate to the CPU the clock cycles when the CPU_DQ bus has valid read-back data. Synchronous to FCU_CPU_CLK</td><td>Connect directly to the configuration controller.</td></tr>
<tr><td>FCU_LOCK</td><td>CFG</td><td>Output</td><td>Active-high status bit to indicate the FCU lock/unlock status</td><td>Connect directly to the configuration controller.</td></tr>
<tr><td>FCU_STATUS_[1:0]</td><td>CFG</td><td>Output</td><td>FCU status bits showing the FCU state<table><tr><th>FCU_STATUS</th><th>State</th></tr><tr><td>00</td><td>fcu_locked</td></tr><tr><td>01</td><td>sync_found</td></tr><tr><td>10</td><td>ID found</td></tr><tr><td>11</td><td>instance ID found / FCU unlocked</td></tr></table></td><td>Connect directly to the configuration controller.</td></tr>
<tr><td>FCU_FLASH_CSN_[3:0]</td><td>CFG</td><td>Output</td><td>Active-low chip select to enable/disable one or more of the attached flash memory devices.For x1 mode, only CSN[0] is used, for x4 mode connect each CSN[3:0] to a flash device</td><td>If x1 mode is used, leave CSN[3:1] unconnected. In x4 mode, connect all four to the individual serial flash devices.</td></tr>
<tr><td>FCU_FLASH_HOLDN</td><td>CFG</td><td>Output</td><td>Active-low hold output to flash memory device(s). This signal is used to pause serial communications between Speedster and the flash device without deselecting the device or stopping the serial clock. Synchronous to FLASH_SCK.</td><td>Connect directly to the configuration controller.</td></tr>
<tr><td>FCU_FLASH_SCK</td><td>CFG</td><td>Output</td><td>Clock output from FCU to flash memory device(s)</td><td>Connect directly to the flash device(s).</td></tr>
</table>

Pin Name	Pin Group	Type	Description	Connection Guidelines
FCU_OSC_CLK	CFG	Output	This clock is internally generated from a ring oscillator. For debug purposes it can be bypassed and the external clock CPU_CLK can be used.	Connect directly to the configuration controller.
General Purpose I/O Interface				
GPIO_[N0/S0]_BYTE[2:0]_VREF	DATA	Input	External reference voltage supply to the GPIO.	Typically set to GPIO_VDDIO/2.
GPIO_[N0/S0]_BYTE[2:0]_ZCAL	DATA	Input	Impedance calibration input, one for each GPIO bank.	Requires an off-chip precision resistor 240Ω ±1% terminated to ground.
GPIO_[N0/S0]_BYTE[2:0]_BIT_[11:0]	DATA	Input /Output	Single-ended GPIOs that support multiple IO standards at multiple voltages. They are grouped into bytes of 12 IOs each. Pseudo differential pairs can be built using two adjacent buffers.	Unused I/Os can be left unconnected.
SerDes				
SRDS_N03_ATEST	SRDS (PCIe_x16_N)	Output	Output pin to probe/force internal analog nodes during system bring-up.	High impedance output. Connect to an observation point on the board.
SRDS_N[3:0]_REFCLK_[N/P]		Clock	SerDes reference clock supplied from either a single-ended or differential external source. There is 1 differential pair for each lane.	Connect these clocks for all SerDes lanes used in the interface. Unused clocks should be tied to their own individual GND via an optional 50Ω ±1% termination resistor. Each SerDes quad has a common reference clock. For PCIe x16 mode, reference clocks for all the SerDes quads need to be connected.
SRDS_N[3:0]_RX_[N/P][3:0]		Input	Receive differential inputs to the SerDes. There is one differential pair per each lane.	Connect unused receive pins to GND via an optional 50Ω ±1% termination resistor.
SRDS_N[3:0]_TX_[N/P][3:0]		Output	Transmit differential outputs from the SerDes. There is one differential pair per each lane.	These pins should be AC coupled. Leave all unused transmit pins unconnected.
SRDS_N47_ATEST		Output	Output pin to probe/force internal analog nodes during system bring-up.	High impedance Output. Connect to an observation point on the board.

Pin Name	Pin Group	Type	Description	Connection Guidelines
SRDS_N[5:4]_REFCLK_[N/P]	SRDS (ETH_N)	Clock	SerDes reference clock supplied from either a single-ended or differential external source. There is 1 differential pair for each lane.	Connect these clocks for all SerDes lanes used in the interface. Unused clocks should be tied to their own individual GND via an optional 50Ω ±1% termination resistor.
SRDS_N[5:4]_RX_[N/P][3:0]		Input	Receive differential inputs to the SerDes. There is one differential pair per each lane.	Connect unused receive pins to GND via an optional 50Ω ±1% termination resistor.
SRDS_N[5:4]_TX_[N/P][3:0]		Output	Transmit differential outputs from the SerDes. There is one differential pair per each lane.	These pins should be AC coupled. Leave all unused transmit pins unconnected.
SRDS_N[7:6]_REFCLK_[N/P]	SRDS (PCIe_x8_ETH_N)	Clock	SerDes reference clock supplied from either a single-ended or differential external source. There is 1 differential pair for each lane.	Connect these clocks for all SerDes lanes used in the interface. Unused clocks should be tied to their own individual GND via an optional 50Ω ±1% termination resistor. If configured to be PCIe compliant x8 mode, reference clocks for all 8 SerDes lanes need to be connected. If configured to operate as non-PCIe compliant x4 mode, the unused lanes' clocks should be tied to their own individual GND via an optional 50Ω ±1% termination resistor.
SRDS_N[7:6]_RX_[N/P][3:0]		Input	Receive differential inputs to the SerDes. There is one differential pair per each lane.	Connect unused receive pins to GND via an optional 50Ω ±1% termination resistor.
SRDS_N[7:6]_TX_[N/P][3:0]		Output	Transmit differential outputs from the SerDes. There is one differential pair per each lane.	These pins should be AC coupled. Leave all unused transmit pins unconnected.
Miscellaneous				
TS_AN_IO_[1:0]	TEMP	Input /Output	Analog I/O pins used for test access and calibration	If the temperature monitoring feature is not used, leave unconnected. Otherwise, connect appropriately to the temperature sensor.
DDR4				
DDR4_S0_A17	IP	Output	Address input to SDRAM (used in x4 configuration only)	Connect to the appropriate signals on the DDR4 DIMM.
DDR4_S0_ACT_N	IP	Output	Active-low ACTIVATE command to SDRAM	

Pin Name	Pin Group	Type	Description	Connection Guidelines
DDR4_S0_A_[13:0]	IP	Output	Bank Address inputs to SDRAM	Connect to the appropriate signals on the DDR4 DIMM.
DDR4_S0_BA_[1:0]	IP	Output	Bank Select Inputs to SDRAM	Connect to the appropriate signals on the DDR4 DIMM.
DDR4_S0_BG_[1:0]	IP	Output	Bank Group inputs to SDRAM	
DDR4_S0_BP_ALERT_N	IP	Input /Output	I/O signal driven by DDR4 SDRAM to signal to the host controller when the SDRAM detects an error on the DDR interface, or, is a signal driven by the host controller to the SDRAM during Connectivity test mode	
DDR4_S0_BP_MEMRESET_L	IP	Output	Active-low memory reset signal to external SDRAM	
DDR4_S0_BP_VREF	IP	Input /Output	Reference Voltage to external SDRAM	
DDR4_S0_BP_ZN	IP	Output	External calibration resistor drive	Supported calibration resistor values are 40Ω, 120Ω and 240Ω ±1%.
DDR4_S0_CAS_N	IP	Output	Active-low column address select signal to external SDRAM. When ACT_N and CS_N are low, these outputs are interpreted as column address bits. When ACT_N is high, these outputs are interpreted as command pins to indicate READ, WRITE or other commands.	Connect to the appropriate signals on the DDR4 DIMM.
DDR4_S0_CID_[2:0]	IP	Output	Chip ID select for stacked components	
DDR4_S0_CKE_[3:0]	IP	Output	SDRAM clock enable control signal	
DDR4_S0_CK_[T/C]_[3:0]	IP	Output	Differential clock inputs to DRAM. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_T and the negative edge of CK_C	
DDR4_S0_CS_N_[3:0]	IP	Output	Active-low chip select signals to external SDRAM. All commands are masked when CS_n is registered HIGH. CS_N provides external rank selection on systems with multiple ranks	

Pin Name	Pin Group	Type	Description	Connection Guidelines
DDR4_S0_UDQS_C_[8:0]	IP	Input /Output	Data Mask and Data Bus Inversion signals to SDRAM	Connect to the appropriate signals on the DDR4 DIMM.
DDR4_S0_DQ_[8:0]_[7:0]	IP	Input /Output	SDRAM data bus	
DDR4_S0_LDQS_[T/C]_[8:0]	IP	Input /Output	SDRAM data strobe signals	
DDR4_S0_ODT_[3:0]	IP	Output	SDRAM on-die termination control signal	ODT resistances can be configured to one of these values (open, 240, 120, 80, 60, 48, 40) pulled up to DDR4_S0_VDDQ.
DDR4_S0_PAR	IP	Output	Command/Address Parity input to SDRAM	Connect to the appropriate signals on the DDR4 DIMM.
DDR4_S0_RAS_N	IP	Output	Active-low row address select signal to external SDRAM. When ACT_N and CS_N are low, these outputs are interpreted as row address bits. When ACT_N is high, these outputs are interpreted as command pins to indicate READ, WRITE or other commands.	
DDR4_S0_DM_DBI_UDQS_T_[8:0]	IP	Input /Output	SDRAM data strobe signals	
DDR4_S0_WE_N	IP	Output	Active-low write enable signal	
GDDR6				
GDDR6_[E/W][3:0]_C[1:0]_SD_CABI_N	IP	Output	Active-low command address bus Inversion input to GDDR6 memory	Connect to the appropriate GDDR6 memory signals.
GDDR6_[E/W] [3:0]_C[1:0]_SD_CA_[9:0]	IP	Output	Command Address inputs to GDDR6 memory	
GDDR6_[E/W] [3:0]_C[1:0]_SD_CKE_N	IP	Output	Active-low clock enable input to GDDR6 memory	
GDDR6_[E/W] [3:0]_C[1:0]_SD_DBI_N_ [1:0]	IP	Input /Output	Active-low data bus inversion inputs to GDDR6 memory	

Pin Name	Pin Group	Type	Description	Connection Guidelines
GDDR6_[E/W] [3:0]_C[1:0]_SD_DQ_[15:0]	IP	Input /Output	Bidirectional data input/output	Connect to the appropriate GDDR6 memory signals.
GDDR6_[E/W] [3:0]_C[1:0]_SD_EDC_[1:0]	IP	Input	Error detection code from GDDR6 memory	
GDDR6_[E/W] [3:0]_C[1:0]_SD_WCK_[N/P]_[1:0]	IP	Output	Differential data clock inputs to memory	
GDDR6_[E/W] [3:0]_RREF	IP	Input	Reference resistor for ZQ calibration	Nominal 240 Ohm to ground ±1% tolerance.
GDDR6_[E/W] [3:0]_SD_CLK_[N/P]	IP	Output	Differential clock inputs to memory	Connect to the appropriate GDDR6 memory signals.
GDDR6_[E/W] [3:0]_SD_RESET_N	IP	Output	Active-low Reset to GDDR6 memory	
GDDR6_E2_ATESTCA	IP	Input	Analog voltage monitor for CA signals	Connect directly to observation point.
GDDR6_E2_ATESTDQL	IP	Input	Analog voltage monitor for lower DQ signals	
GDDR6_E2_ATESTDQR	IP	Input	Analog voltage monitor for higher DQ signals	
GDDR6_W1_ATESTCA	IP	Input	Analog voltage monitor for CA signals	
GDDR6_W 1_ATESTDQL	IP	Input	Analog voltage monitor for lower DQ signals	
GDDR6_W 1_ATESTDQR	IP	Input	Analog voltage monitor for CA signals	

Chapter - 3: Revision History

Version	Date	Description
1.0	24 May 2019	• Initial Achronix release.
1.1	11 Jun 2019	• Removed double prefixes from FCU, JTAG and TS pin names. • Renamed UDQS_T signals in DDR4 interface to DM_DBI_UDQS_T and DM_DBI_UDQS_C signals to UDQS_C. • Updated FCU Io pins to include strap signals, stap_sel and error status signals • Updated GDDR6 ATEST signals for the East and West sides.