Speedster7t FPGA Datasheet (DS015)

Speedster FPGAs

Preliminary Data

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Data Acceleration

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Preliminary Data

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Chapter - 1: Overview

Introducing the Speedster7t FPGA Family

The Achronix high-performance, 7nm Speedster®7t FPGA family is specifically designed to support extremely high bandwidth requirements for demanding applications including data-center workloads and networking infrastructure. The processing tasks associated with these high-performance applications, specifically those associated with artificial intelligence and machine learning (AI/ML) and high-speed networking, represent some of the most demanding processing workloads in the data center.

Several performance criteria characterize these data-center and networking workloads requiring the following abilities:

- Handle high-speed data rates from a host processor PCIe Gen5 port and up to 400 Gbps on the Ethernet ports
- Store multiple gigabytes of incoming data and to access that data quickly for processing within the FPGA
- Move massive amounts of data among the FPGA I/O ports, its internal memory, attached external memory, and its on-chip computing resources
- Process high computational workloads with tera operations per second (TOPS) performance.

The Speedster7t FPGA family can more than satisfy each of these performance criteria with appropriately scaled and optimized on-chip resources.

Handling High-Speed Incoming and Outgoing Data

For data center and networking applications, high-speed data enters an FPGA-based processing node in two fundamental ways: through PCIe connections to a host processor and via high-speed Ethernet connections. The Speedster7t FPGA family is designed to maximize data rates over these connections by implementing a number of PCIe Gen5 interfaces for the host processor connection(s) and multiple SerDes ports capable of supporting 400 Gbps Ethernet connections. Both of these I/O standards represent the fastest, most recent specifications for inter- and intra-system data communications used in data centers and myriad other FPGA-based applications.

Fast, High-Capacity Memory Storage

Most FPGAs store data that must be accessed quickly in on-chip SRAM. The Speedster7t FPGA family is no exception, incorporating a substantial amount of on-chip memory. However, the sheer volume of data that must be handled by many data center applications often outpaces the available amount of on-chip SRAM, even when the FPGA in question is fabricated with 7nm FinFET process technology.

Consequently, the Speedster7t FPGA is designed with multiple GDDR6 SDRAM ports. GDDR6 SDRAMs provide the fastest SDRAM access speeds with the lowest DRAM cost (per stored bit). Together, these characteristics make GDDR6 SDRAM interfaces the best choice for next-generation system designs. Members of the Speedster7t FPGA family support as many as eight independent GDDR6 memory ports.

Massive On-Chip Data Movement

With multiple high-speed PCIe Gen5 and 400 Gbps Ethernet ports combined with GDDR6 SDRAM interfaces, the Speedster7t FPGA family can move a tremendous amount of data directly between these various I/O ports and to the FPGA on-chip memory and computational resources. Speedster7t FPGAs employ both the familiar parallel interconnections of earlier FPGA generations and a new 2D network on chip (2D NoC) to facilitate the significantly faster data transfer rates required by future data centers applications. The 2D NoC provides over 20Tbps of data bandwidth within the FPGA device resources and I/O interfaces.

Consider 400 Gbps Ethernet ports, which require a 724 MHz, 1024-bit internal bus within an FPGA to handle a single, full bandwidth, bidirectional 400 Gbps data stream. This wide bus is extremely difficult to route in a conventional FPGA switching fabric based on internal, parallel connections. Now, consider the need to handle multiple 400 Gbps Ethernet ports within a single FPGA — the requirements become even tougher. These are the sorts of data rates that the Speedster7t FPGA on-chip 2D NoC is designed to handle with ease.

High-speed, On-Chip Processing Resources

FPGAs excel at processing data at high-speeds due to their configurable logic and co-located SRAM resources. The Speedster7t FPGA family includes the same processing resources and memories found in previous generation FPGAs, but adds optimizations and new processing elements to further enhance performance for many applications, including AI/ML applications.

For example, Speedster7t FPGAs incorporate new resources called machine learning processor (MLP) blocks, which are large-scale, matrix-vector and matrix-matrix multiplication engines specifically designed to accelerate AI /ML applications. MLP blocks support fixed and floating-point computations and their resources are fracturable to support the wide range of numerical precision employed by AI/ML applications.

The MLP block architecture has been designed to exploit data reuse opportunities that are inherent to matrix-vector and matrix-matrix multiplication. This data reuse significantly reduces the amount of data movement among memories, which increases AI/ML algorithm performance while cutting power consumption. In addition, multipliers implemented with the Speedster7t FPGA lookup tables (LUTs) have been reformulated with the industry's most efficient modified Booth's algorithm, which doubles LUT-based multiplier performance for AI/ML algorithms.

Feature Summary

- Two-dimensional network on chip (2D NoC) enabling high bandwidth data flow throughout and between the FPGA fabric and hard I/O and memory controllers and interfaces
- MLP blocks with arrays of multipliers, adder trees, accumulators, and support for both fixed and floating point operations
- Multiple PCIe Gen5 ports
- High-speed SerDes transceivers, supporting 112 Gbps PAM4 and 56 Gbps PAM4/NRZ modulation, as well as lower data rates
- Hard Ethernet MACs that support up to 400 Gbps
- GDDR6 and DDR5 SDRAM controllers and interfaces (the Speedster7t AC7t1500 supports DDR4 rather than DDR5)
- Fabric-based bi-directional cryptographic engine (Speedster7t AC7t1550)
- Hard bi-directional cryptographic engine (Speedster7t AC7t800)
- New logic architecture with 6-input LUTs (6LUT), 8-bit ALUs, flip-flops, and a reformulated multiplier LUT (MLUT) mode based on a modified Booth's algorithm, which doubles the performance of LUT-based multiplication
- Fabric routing enhanced with dedicated bus routing and active bus muxing
- 72 kb BRAM and 2 kb LRAM memory blocks
- GPIO supporting multiple I/O standards
- PLLs and DLLs to support multiple, on-chip clock trees
- Support for multiple types of programming interfaces
- Partial reconfiguration of the FPGA fabric
- Remote update of the FPGA fabric
- Security features for encrypting and authenticating bitstreams
- Debug support through Achronix Snapshot

Family Features

Table 1: ***Speedster7t FPGA Family Overview***

Part Number/Name	AC7t800	AC7t1500	AC7t1550
6-input LUTs	326k	692k	606k
Inline Cryptography	Yes	No	Yes
MLP: Multi-fracturable MAC array	864	2,560	2,240
LRAM (2.3 kb)	864	2,560	2,240
BRAM (73.7 kb)	1,152	2,560	2,240
Memory	85 Mb	190 Mb	166 Mb
ML TOps: int8 or block bfloat16	20.5	61	53
SerDes 112G/224G	24	32	
DDR4/5	1 DDR5 ×64 (w/ ECC)	1 DDR4 ×64 (w/ ECC)	
High-bandwidth memory channels	6 GDDR6 (1.5 Tbps, w/ ECC)	16 GDDR6 (4 Tbps)	
PCI Express Gen5	One ×16	One ×8, one ×16	
Ethernet	8 lanes, 2×400G/ 8×100G	16 lanes, 4×400G/ 16×100G	
2D NoC bandwidth (Tbps)	12	20	

Table 2: ***Speedster7t FPGA Package and I/O Combinations***

Package Dimensions (mm)	AC7t800	AC7t1500/AC7t1550
	GDDR6, SerDes, GPIO	**GDDR6, SerDes, GPIO**
45×45	6 channels, 24, 32	–
52.5×52.5	–	16 channels, 32, 64

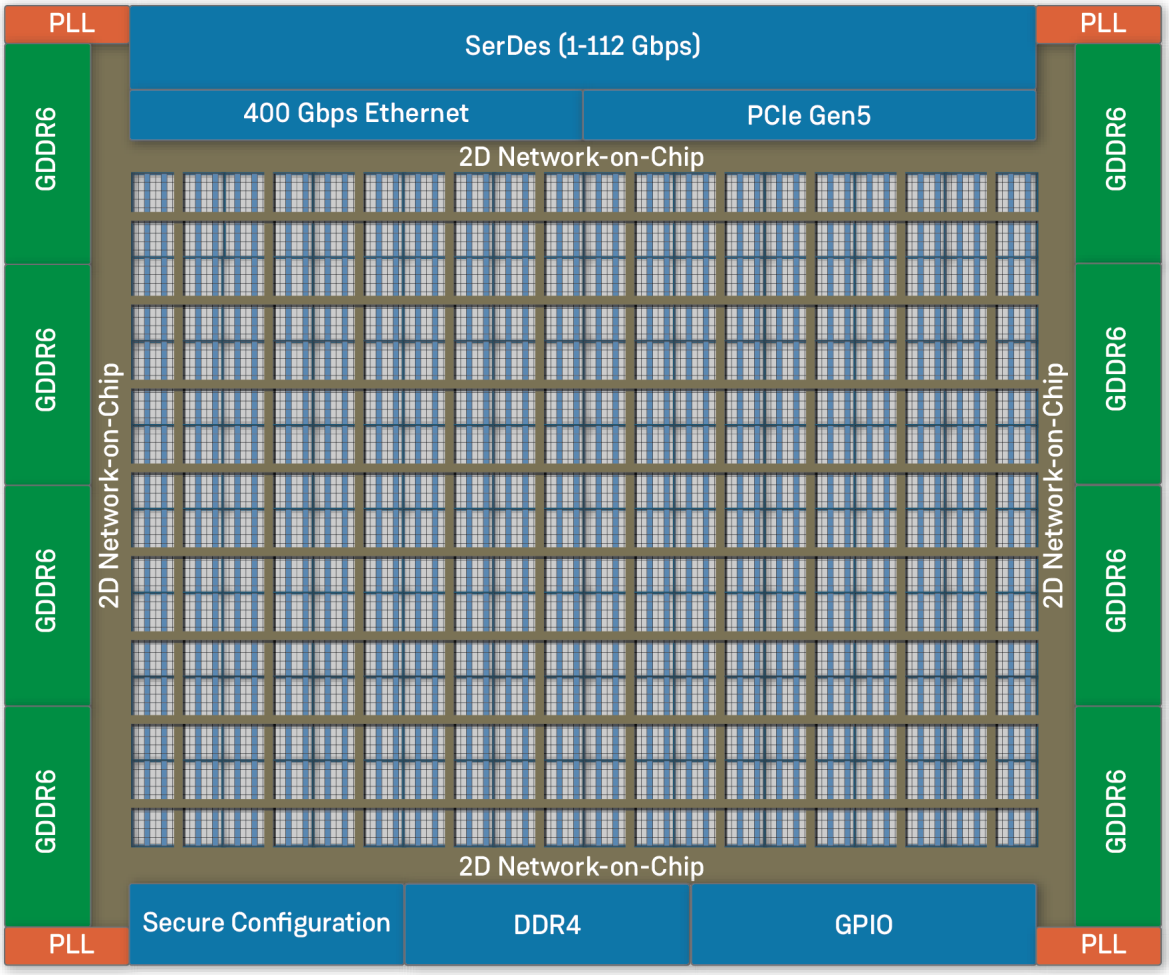


Figure 1: ***Speedster7t AC7t1500 Top-Level Block Diagram***

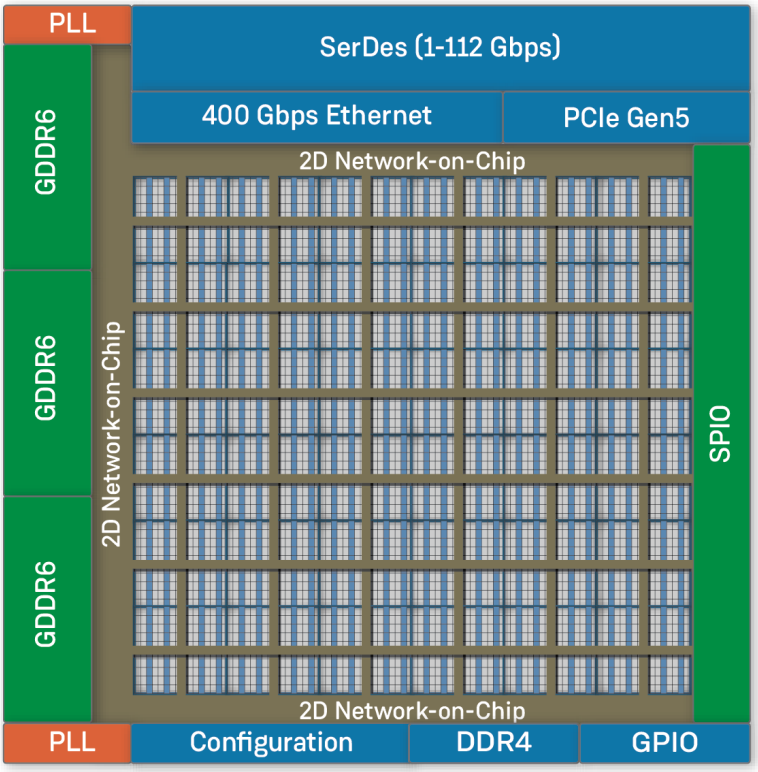


Figure 2: ***AC7t800 Top-Level Block Diagram***

Chapter - 2: Speedster7t Fabric Architecture

The Speedster7t FPGA fabric is optimized for artificial intelligence and machine learning applications as well as hardware acceleration. The fabric is comprised of up to three main tile types:

- Reconfigurable logic blocks (RLBs) containing look-up tables, flip-flops, and ALUs
- Machine learning processor (MLP) blocks containing multipliers, adders, accumulators, and tightly-coupled memory (includes BRAM72k and LRAM2k)
- In the Speedster7t AC7t800, standalone Block RAM 72k (BRAM72k) memory blocks

The tiles are distributed as columns in the Speedster7t FPGA, and each tile consists of a routing switch box plus a logic block.

Fabric Clusters

Speedster7t FPGA fabric is constructed by arranging rows and columns of tiles into a basic unit of layout called a fabric cluster. The complete fabric in a device is created by replicating the fabric clusters into a larger grid of rows and columns. All fabric clusters are identical, containing exactly the same pattern of tile rows and columns, with an initiator and responder network access point (NAP) in the center. The exact numbers of fabric clusters, the dimensions of each cluster, and the arrangement and types of tiles within each cluster, are specific per device. For example, the Speedster7t AC7t1500 has 8 rows and 10 columns of fabric clusters, for a total of 80. The following figure shows the fabric clusters:

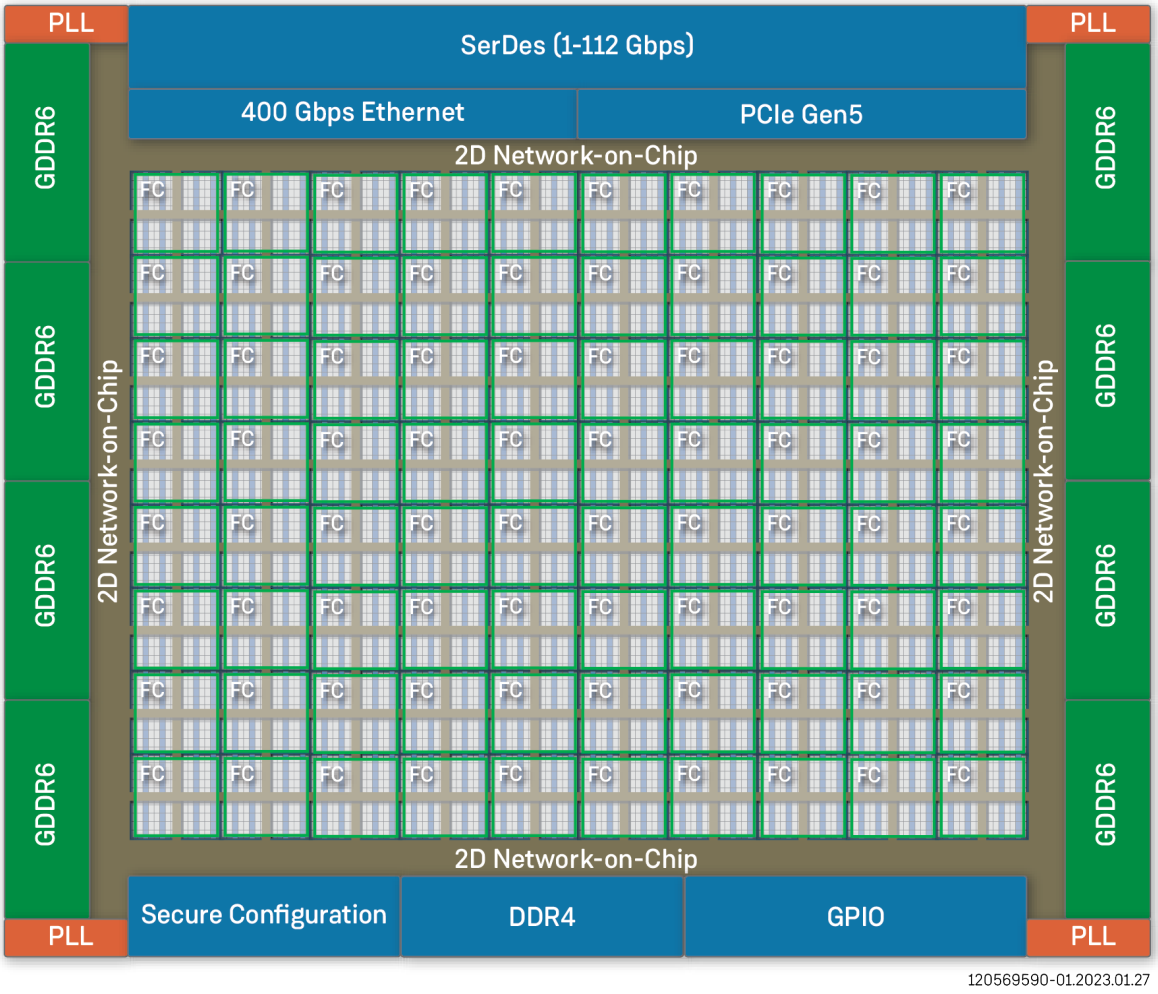


Figure 3: ***Fabric Clusters on the Speedster7t AC7t1500 FPGA***

While fabric cluster boundaries are otherwise transparent to a user, a designer can make use of this regularity of fabric clusters if the design consists of a number of identical cores. If the cores are designed to fit within one or more fabric clusters, a complete design can be created by replicating that core multiple times across the device using the fabric cluster grid. Additionally, the fabric cluster structure along with the NAP in the center of each cluster provide support for partial reconfiguration. The NAP provides a path to route signals on and off the NoC in the center of the cluster, and the regularity of the cluster makes it easy for multiple cores to be configured for the same cluster space.

Fabric Clock Network

Speedster7t FPGAs have two types of clock networks targeted to provide both a low-skew and a balanced architecture, as well as addressing the source-synchronous nature of data transfers with external interfaces:

1. The global clock network is the hierarchical network that feeds resources in the FPGA fabric. The global clock trunk runs vertically up and down the center of the core, sourced by global clock muxes at the top and bottom of the global trunk. The global clock network uses low-latency and low-skew distribution techniques to reach all possible endpoints in the FPGA fabric.
2. The interface clock network, available at the periphery of the fabric, facilitates the construction of interface logic within the FPGA fabric operating on the same clock domain as external logic. Specifically, interface clocks drive the logic that communicates with the hard IP interfaces on a Speedster7t FPGA. Interface clocks are optimized for low latency and drive logic within a specific area in the FPGA fabric.

Achronix provides dedicated clock dividers, glitchless clock switches, and clock gates for ease of use in a customer design. Additionally, ACE automatically provides support for inserting programmable delays at various points on a clock path to increase performance and easily facilitate timing closure.

Fabric Routing

Global Interconnect

All tiles in the fabric are connected through the global interconnect, allowing for routing between elements e.g., RLBs, MLPs, BRAMs, etc. Switchboxes in each tile act as the connection points between vertical and horizontal routing tracks. In addition to the traditional per-signal routing, the Speedster7t FPGA family introduces bus routing for high-performance data paths.

Bus Routing

The Speedster7t FPGA includes both traditional per-bit routing, as well as dedicated bus routing. The Speedster7t FPGA architecture includes separate dedicated bus-based routing for high-performance datapaths. These buses are placed into groups of up to 8 bits wide and are routed independently from standard routing in order to significantly reduce congestion.

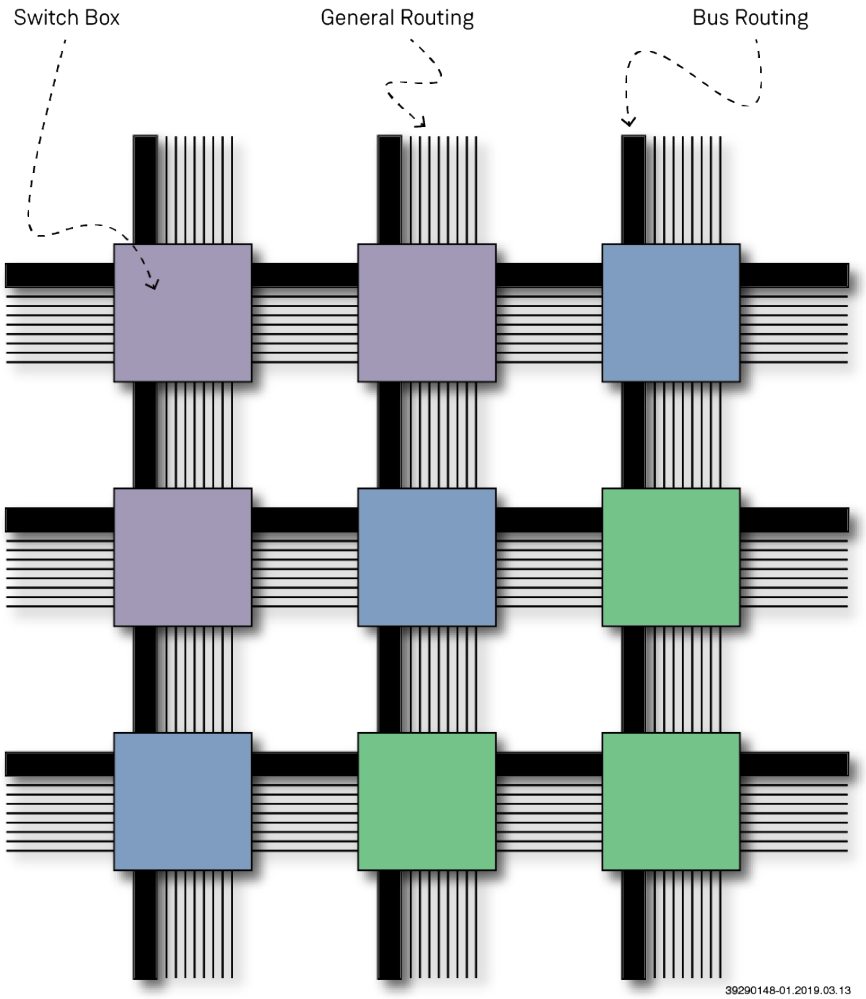


Figure 4: ***Speedster7t Bus Routing***

Additionally, the Speedster7t FPGA architecture introduces a programmable switch network for bus routing. Four 8-bit buses, one from each direction, enter each Speedster7t switchbox. Additionally, there is a 4 × 1 bus MUX for each of the 8-bit buses inside the switchbox. These bus MUXes are cascadable for wider muxing requirements. This added muxing reduces overall logic and routing resources for a design, leading to improved performance and smaller area.

Reconfigurable Logic Block (RLB)

An RLB contains 6-input look-up-tables (LUT6), a number of registers, and 8-bit fast arithmetic logic units (ALU8). The following table provides information on the resource counts inside an RLB in the Speedster7t FPGA.

Table 3: *RLB Resource Counts*

Resource	Count
LUT6	12
Registers	24
8-bit ALU	3

The following features are available using the resources in the RLB:

- 8-bit ALU for adders, counters, and comparators
- 8-to-1 MUX with single-level delay (can be inferred)
- Support for LUT chaining within the same RLB and between RLBs
- Dedicated connections for high-efficiency shift registers
- Multiplier LUT (MLUT) mode for efficient multipliers (for Speedster7t devices only)
- Ability to fan-out a clock enable or reset signal to multiple tiles without using general routing resources
- 6-input LUT configurable to function as two 5-input LUTs using shared inputs and two outputs
- Support for combining two 6-input LUTs with a dynamic select to provide 7-input LUT functionality

MLUT Mode

The RLB includes an MLUT mode for an efficient LUT-based multiplication. MLUT mode results in 2 × 2 multiplier building blocks that can be stacked horizontally and vertically to generate any size signed multiplier. For example, a 2 × 4 multiplier building block can be generated with two LUT6s, and one RLB can perform a 6 × 8 multiply.

Note

MLUT mode is supported by the MLUT generator within ACE to help build the desired multiplier.

Machine Learning Processor (MLP) Block

The machine learning processor block (MLP) is an array of up to 32 multipliers, followed by an adder tree, and an accumulator. The MLP is also tightly coupled with two memory blocks, a BRAM72k and LRAM2k. These memories can be used individually or in conjunction with the array of multipliers. The number of multipliers available varies with the bit width of each operand and the total width of input data. When the MLP is used in conjunction with a BRAM72k, the number of data inputs to the MLP block increases, enabling the use of additional multipliers.

The MLP offers a range of features:

- Configurable multiply precision and multiplier count. Any of the following modes are available:
  - Up to 32 multiplies for 4-bit integers or 4-bit block floating-point values in a single MLP
  - Up to 16 multiplies for 8-bit integers or 8-bit block floating-point values in a single MLP
  - Up to 4 multiplies for 16-bit integers in a single MLP
  - Up to 2 multiplies for 16-bit floating point with both 5-bit and 8-bit exponents in a single MLP
  - Up to 2 multiplies for 24-bit floating point in a single MLP
- Multiple number formats:
  - Integer
  - Floating point 16 (including B float 16)
  - Floating point 24
  - Block floating point, a method that combines the efficiency of the integer multiplier-adder tree with the range of the floating point accumulators
- Adder tree and accumulator block
- Tightly-coupled register file (LRAM) with an optional sequence controller for easily caching and feeding back results
- Tightly-coupled BRAM for reusable input data such as kernels or weights
- Cascade paths up a column of MLPs
  - Allows for broadcast of operands up a column of MLPs without using up critical routing resources
  - Allows for adder trees to extend across multiple MLPs
  - Broadcast read/write to tightly-coupled BRAMs up a column of MLPs to efficiently create large memories

Along with the numerous multiply configurations, the MLP block includes optional input and pipelining registers at various locations to support high-frequency designs. There is a deep adder tree after the multipliers with the option to bypass the adders and output the multiplier products directly. In addition, a feedback path allows for accumulation within the MLP block.

The following block diagrams show the MLP using the fixed or floating-point formats:

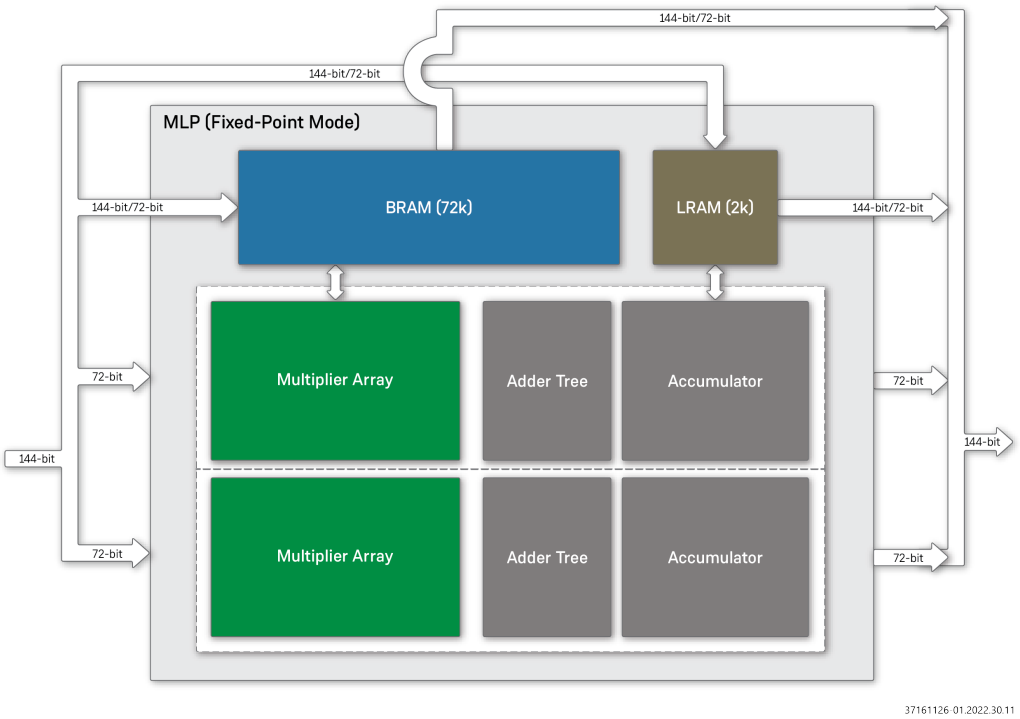


Figure 5: ***MLP Using Fixed-Point Mode***

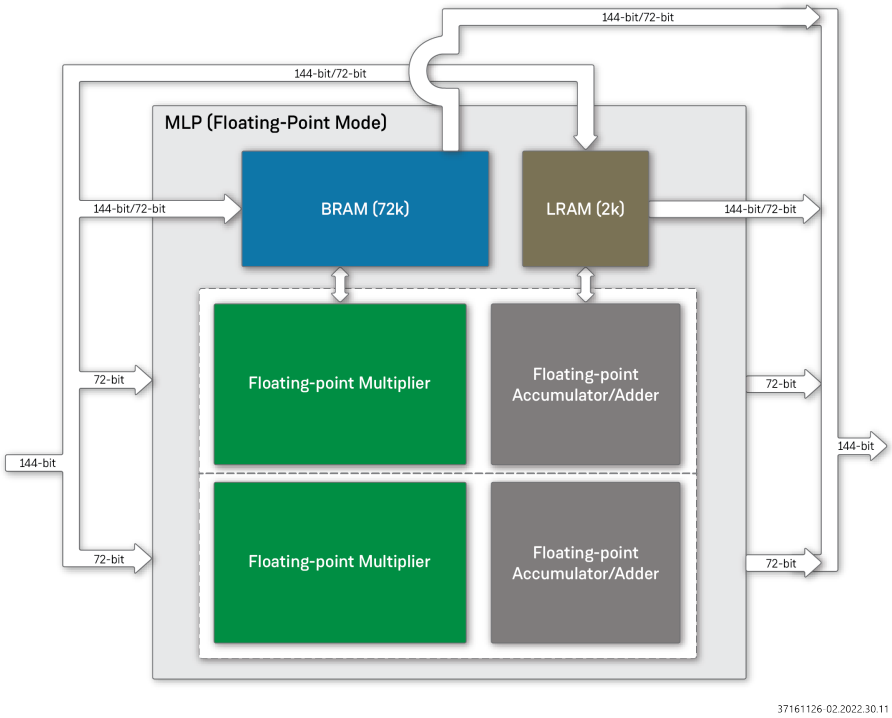


Figure 6: ***MLP Using Floating-Point Mode***

A powerful feature available in the Achronix MLP is the ability to connect several MLPs with dedicated high-speed cascade paths. The cascade paths allow for the adder tree to extend across multiple MLP blocks in a column without using extra fabric routing resources, and a data cascade/broadcast path is available to send operands across multiple MLP blocks. Cascading input or result data to multiple MLPs in parallel allows for complex, multi-element operations to be performed efficiently without the need for extra routing. The following diagram shows the cascade paths across MLPs:

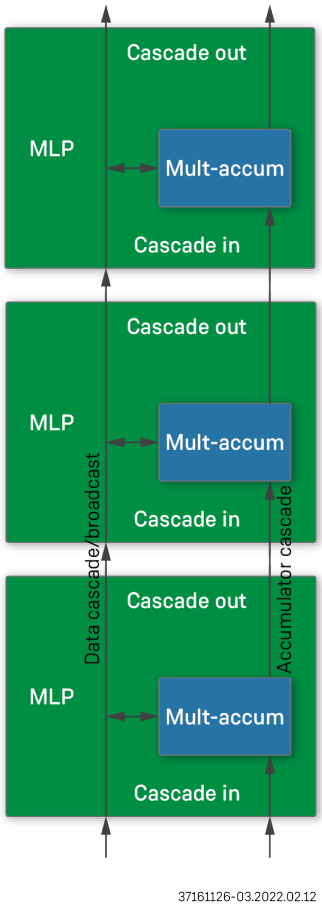


Figure 7: ***MLP Cascade Path***

Block RAM 72k (BRAM72k)

The BRAM72K primitive implements a 72Kb simple-dual-port (SDP) memory block with one write port and one read port. Each port can be independently configured with respect to size and function, and can use independent read and write clocks. The BRAM72K can be configured as a simple dual port or ROM memory. The key features (per block RAM) are summarized in the following table:

Table 4: *BRAM72K Key Features*

Feature	Value
Block RAM size	72Kb
Organization	512 × 144, 128 × 512, 1024 × 72, 1024 × 64, 2048 × 36, 2048 × 32, 4096 × 18, 4096 × 16, 8192 × 9, 8192 × 8, or 16384 × 4
Physical Implementation	Columns throughout device
Number of Ports	Simple Dual Port (independent read and write)
Port Access	Synchronous writes, synchronous reads (write and read clocks can be asynchronous to each other)
FIFO	Built-in FIFO controller with dedicated pointer and flag circuitry

The BRAM72K ports are Illustrated in the following figure:

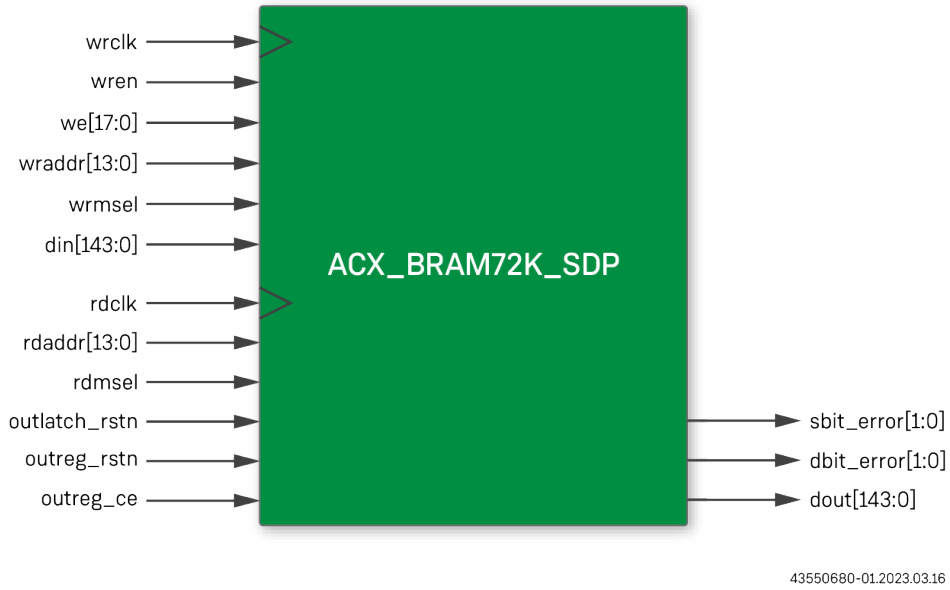


Figure 8: *BRAM72K Block Diagram*

Logic RAM 2k (LRAM2k)

The LRAM2K implements a 2,304-bit memory block configured as a 32 × 72 simple dual-port (one write port, one read port) RAM. The LRAM2K has a synchronous write port. The read port is configured for asynchronous read operations with an optional output register. A summary of LRAM2K features is shown in the following table:

Table 5: *LRAM2K Key Features*

Feature	Value
Logic RAM size	2,304 bits
Organization	16 × 144, 32 × 72 or 64 × 36 (depth × width)
Physical Implementation	Columns throughout device
Number of Ports	Simple dual port (one read, one write)
Port access	Synchronous writes, combinatorial reads
FIFO	Built-in FIFO controller with dedicated pointer and flag circuitry

The LRAM2K ports are shown in the following figure:

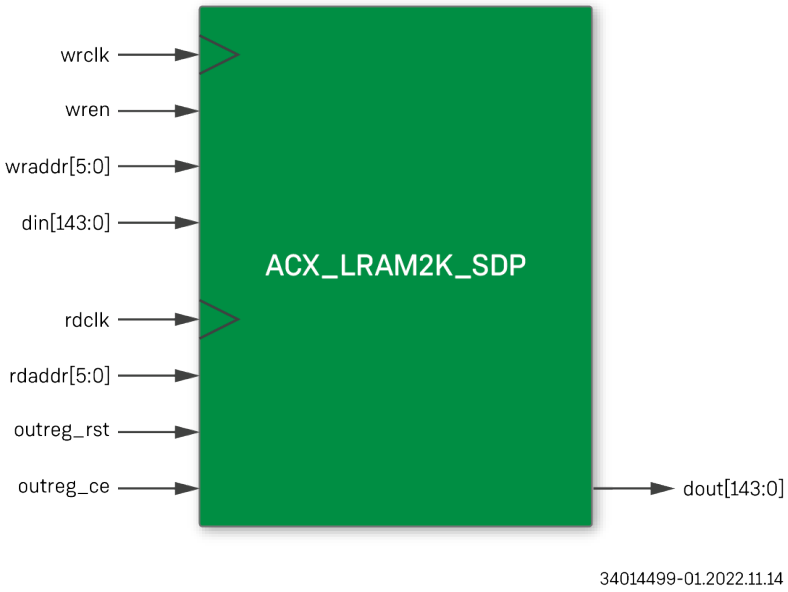


Figure 9: *LRAM2K Block Diagram*

Chapter - 3: Speedster7t FPGA I/O and PHY

Speedster7t FPGAs have a variety of I/O and PHY to communicate with external components.

112 Gbps SerDes

Speedster7t FPGAs provide high-speed serial transceivers (SerDes) which can be used for interface protocols running from 1 Gbps up to 112 Gbps. The SerDes are designed to support NRZ and PAM4 data center standards. The Speedster7t FPGA provides a PCS and PMA to support the needs of many common high-speed serial protocols.

PMA Features

- Data rates from 1 Gbps to 112 Gbps
- DC coupling or external AC coupling
- Lock to reference clock or data
- Support for oversampling
- BIST with near/far-end loopback and PRBS 7, 13, 15, 23, 31 generator/checker
- Eye monitor

PCS Features

- Data rates from 10 Gbps to 106 Gbps using Ethernet subsystem, 1 Gbps to 64 Gbps raw SerDes
- Supports data path widths of 16, 20, 32, 40, 64, and 128 bits (not all data widths are supported at all data rates)
- 8b/10b encoding/decoding support for PCIe 40-bit internal data paths
- Comma detection and byte/word alignment for PCIe 8b/10b
- 128b/130b encoding/decoding support for PCIe Gen3/Gen4/Gen5 32-bit internal data path
- Elastic receive buffer for clock compensation and channel bonding
- Support for 66b/64b CAUI gearbox in both synchronous and asynchronous mode
- Support for 67b/64b gearbox in synchronous mode
- Native support for Ethernet 10G/25G/50G/100G, XAUI, CPRI, Jesd4C, SyncE, and Interlaken
- Bypass mode for PCS (bypasses the PCS)

GPIO

Speedster7t FPGAs provide general-purpose I/O (GPIO) pins to enable communication with external components. These GPIO support multiple I/O standards at multiple voltages.

The following table lists the supported I/O standards. There are separate clock I/O banks, which are described in the next section.

Table 6: ***Supported General-purpose I/O Standards***

I/O Standard Supported	Supported Voltage (V)	Single-Ended/Differential
HSTL Class I	1.8	single-ended, differential
HSUL	1.2	
LVCMOS	1.1	
	1.2	
	1.35	
	1.5	
	1.8	
SSTL Class I	1.2	
	1.35	
	1.5	
	1.8	
SSTL Class II	1.8	

Special-Purpose I/O (SPIO)

The DDR subsystem in a Speedster7t FPGA can be utilized in two modes: PHY bypass or regular. In the PHY bypass mode where the DDR interface is not being used, all DDR I/O can be accessed as special-purpose I/O. The DDR I/O can be utilized either in regular PHY mode for DDR memory interfacing or in PHY bypass mode, but a combination of the two is not allowed. The SPIO:

- Can drive low-frequency interfaces running at a maximum of 100 Mhz.
- Are not compliant with specific industry I/O standards. These I/O operate at 1.2V (±5%).
- Maintain the signal direction of the DDR interface.
- Can supply up to 157 additional I/O.

Clock I/O

Speedster7t FPGAs provide two types of clock I/O pins to enable communication with external components:

- Multi-standard I/O (MSIO) – clock I/O that support multiple I/O standards at multiple voltages, including pseudo-differential.
- Reference clock differential I/O (REFIO) – clock I/O that support LVCMOS, LVDS, and LVPECL.

The following table lists the supported I/O standards for each clock I/O type.

Table 7: *Supported Clock I/O Standards*

I/O Standard Supported	Supported Voltage (V)	Single-Ended/Differential
MSIO		
HSTL Class I	1.5	single-ended, differential
	1.8	
HSTL Class II	1.5	
LVCMOS	1.5	
	1.8	
SSTL Class I	1.5	
	1.8	
SSTL Class II	1.8	
REFIO		
LVCMOS	1.5	single-ended, differential
	1.8	
LVDS	1.5	differential
	1.8	
LVPECL	1.5	
	1.8	

PLLs

There are sixteen general purpose PLLs, four in each corner of the Speedster7t FPGA. They are fractional-N divide and spread-spectrum PLLs, supporting a wide range of frequencies with excellent jitter performance. The general-purpose PLLs can be used to drive low-skew, high-speed clocks to nearby I/O, the global clock network, and interface clocks in the FPGA fabric.

Available features in the PLLs are:

- Programmable PLL with fractional-N divide and spread-spectrum clock generation
- Wide range of output frequencies supported: 7.5MHz to 2GHz
- Reference clock from dedicated clock I/O, adjacent PLLs (for cascading PLLs), as well as PLLs from other device corners
- Up to four output clocks
- Reference clock and output clock dividers
- Inner and outer bypass paths
- Output duty cycle 50%
- Low jitter
- Low power

Table 8: *PLL Details*

Parameter	Min	Max	Units
Reference frequency	5	600	MHz
Output frequency	7.5	2000	MHz
Maximum long-term jitter	±1% divided reference clock		

DLLs

In each corner of a Speedster7t FPGA there is one initiator DLL with eight targets available for the phase shifting of clocks. This arrangement allows for one initiator clock and up to eight target clocks that can be phase-shifted based on the initiator clock frequency.

> **Note**
>
> The phase-shifted outputs of the DLL can only be routed to the core fabric and not to a CLKIO pin.

The programmable DLLs provide precise phase alignment between output clocks, deskew signals relative to a clock, and includes features such as spread-spectrum support. The DLLs are configured along with the PLLs located in the same corner of the device. Features supported in the programmable DLLs are:

- Supports 300-1333 MHz
- 256 taps
- Lock detection
- Power-down mode when not used in the design
- Supports holding DLL in reset
- Available output test clock
- Control and status register read back

Chapter - 4: Speedster7t FPGA Two-Dimensional Network on Chip

The Speedster7t family of FPGAs has a network hierarchy that enables extremely high-speed data flow between the FPGA core and the interfaces around the periphery as well as between logic within the FPGA itself. This on-chip network hierarchy supports a cross-sectional bidirectional bandwidth exceeding 20 Tbps. It supports a multitude of interface protocols including GDDR6, DDR4/5, 400G Ethernet, and PCI Express Gen5 data streams while greatly simplifying access to memory and high-speed protocols. The Achronix two-dimensional network on chip (2D NoC) provides for read/write transactions throughout the device as well as specialized support for 400G Ethernet streams in selected columns.

Initiator Endpoints

- Up to 80 2D NoC access point (NAP) responders distributed throughout the FPGA core responding to the user-implemented initiator logic endpoint
- All PCI Express Interfaces
- FPGA configuration unit (FCU)

Responder Endpoints

- Up to 80 NAP initiators distributed throughout the FPGA core communicating with the user-implemented responder logic endpoint
- Up to 16x GDDR6 memory interfaces
- DDR4/5 controller
- All PCI Express Interfaces
- All control and status register (CSR) interfaces of all subsystem cores
- FCU (enables configuring of FPGA and interface subsystems)

Packet Endpoints

- Up to 80 vertical and 80 horizontal NAP packet interfaces distributed throughout the FPGA core for fabric-to-fabric transactions
- Up to 32 of the 80 vertical NAPs can send and receive data to/from the Ethernet subsystems, each Ethernet controller connects to two dedicated 2D NoC columns
- Up to two Ethernet subsystems, supporting a mix of up to 4× 400 Gbps Ethernet or 16× 100 Gbps Ethernet

2D NoC Features

The 2D NoC provides a method to easily connect high-bandwidth interfaces to the FPGA fabric, as well as enabling communication between memory and high-speed protocols. To make these high-bandwidth connections both flexible and easy to use, the 2D NoC provides the following features.

Table 9: *2D NoC Features*

Feature Summary	Feature Description
2D NoC Interface Modes	The 2D NoC-to-FPGA access point (NAP) supports the following modes: • AXI 256b responder mode • AXI 256b initiator mode • Ethernet and NAP-to-NAP data streaming mode
2D NoC Address Decoding	The 2D NoC has a global address map and handles all address decoding on transactions, making it easy to send transactions from one endpoint to another.
2D NoC Memory Address translation and Firewall	The 2D NoC implements an address translation table for each NAP. This table allows the FPGA design to control how the global memory space is arranged for each NAP, and allows access to specific memory regions to be blocked for security, also on a per-NAP basis.
2D NoC Forwarding Latency	1 to 3.5 ns of latency from one NAP to the next on the same row or column respectively.
2D NoC Flow Control	The 2D NoC manages flow control internally, such that data is never dropped. Priority NAP weights may be configured to regulate the round-robin flow control which affects congestion and latency.

The 2D NoC extends both vertically and horizontally until reaching the edges of the device. The following diagram shows the Speedster7t AC7t1500 connections between the peripheral portion of the 2D NoC, the high-bandwidth interfaces, and the columns and rows of the 2D NoC. As shown, the Ethernet has dedicated connections of up to 400G to specific columns of the 2D NoC. The PCIe ×16 and ×8 connect to the periphery of the 2D NoC at 512 Gbps and 256 Gbps respectively. For GDDR6, the 2D NoC can achieve bandwidth of up to 2 Tbps over the full group of GDDR6 interfaces on each side of the FPGA. The columns and rows of the 2D NoC can move traffic to/from the user logic in the fabric at up to 512 Gbps in each direction.

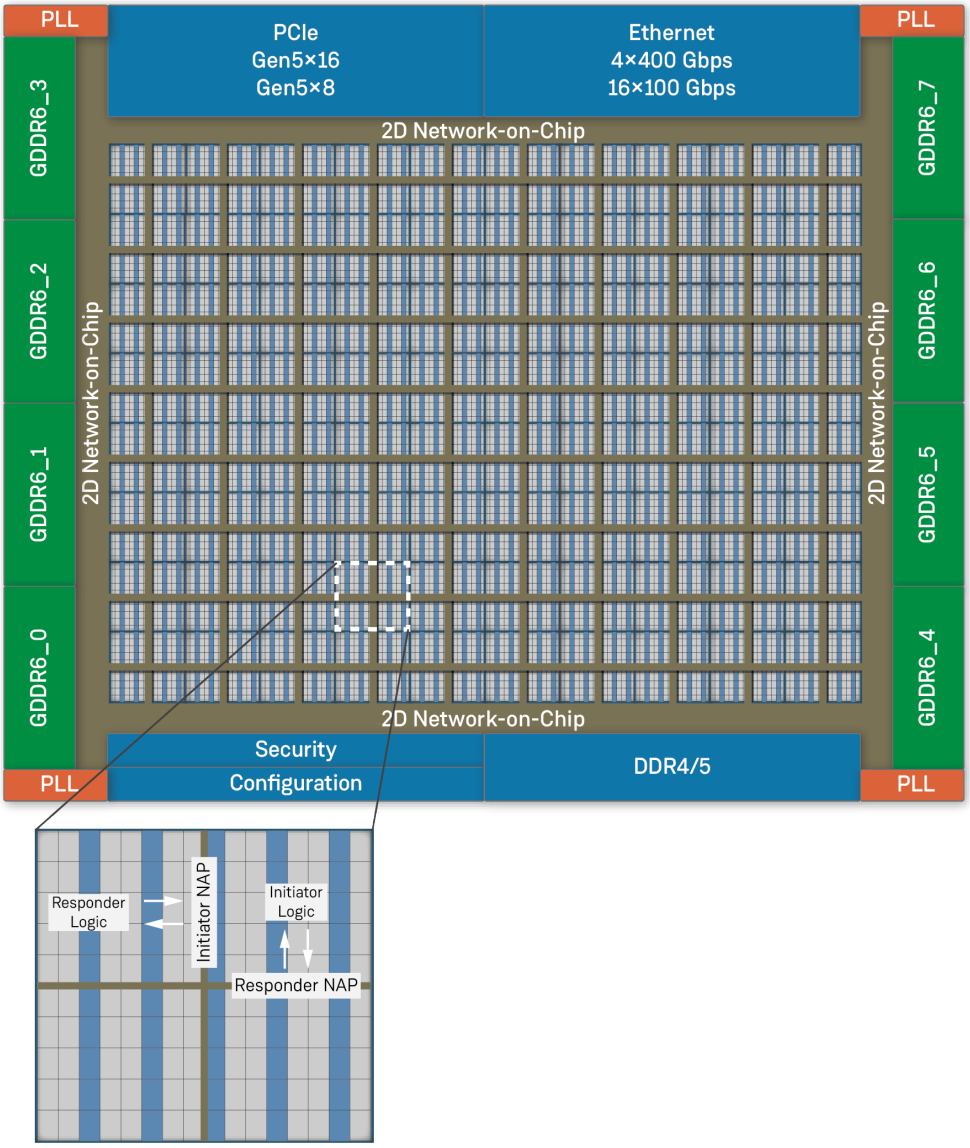


Figure 10: ***Speedcore7t AC7t1500 2D NoC Showing Initiator and Responder Endpoints***

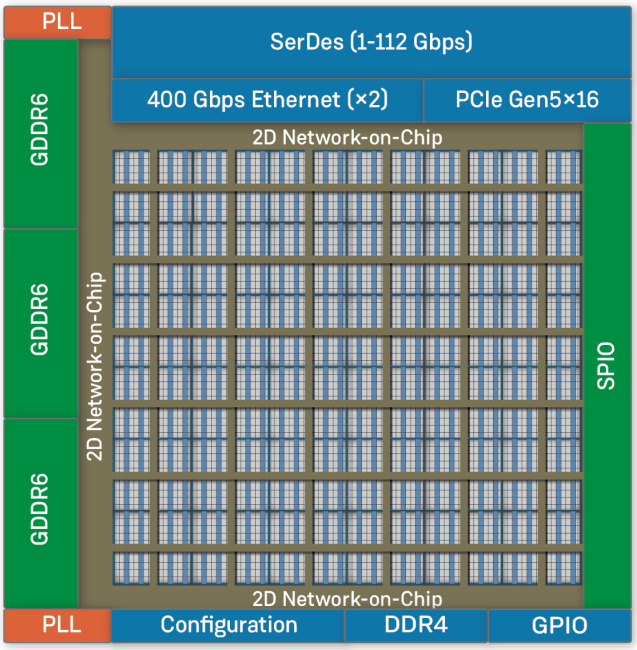


Figure 11: ***Speedcore7t AC7t800 2D NoC***

Columns and Rows of the 2D NoC

The 2D NoC is composed of regularly-spaced node elements at the center of each cluster throughout the core fabric of the FPGA. The 2D NoC nodes provide connectivity to adjacent nodes in both the horizontal and vertical directions. Each horizontal and vertical link within the 2D NoC supports 512 Gbps throughput in both directions.

The 2D NoC transaction mapping logic is optimized for AXI read and write transactions. User initiator logic implemented in the FPGA core can issue AXI read or write transactions to the NAP AXI responder, and the 2D NoC row carries the transaction to the east or west boundary of the FPGA core to be issued to the deep DDR4/5 memory interface or one of the high-speed GDDR6 memory interfaces. PCIe transactions arriving from the north side of the device are issued to the 2D NoC columns, which transport the transaction requests down the columns to user responder logic in the FPGA.

Each row and column can support a full 512 Gbps of traffic.

The rows and columns of the 2D NoC support both transactional and non-transactional data transfers such as streams of data.

- **Transactional data transfer** – this type of transfer includes AXI read and write commands, data, and responses. The command transfers are typically a single cycle, and data transfers are typically one or more cycles, depending on the length of the burst.

- **Non-transactional data transfer** – this type of transfer pushes data streams through the 2D NoC as in a FIFO. A point-to-point data transfer, it is used in two types of transfers:
  - Ethernet – this transfer allows data to be bundled as longer streams of data. Data is sent down selected columns from Ethernet to a specific NAP on the column.
  - NAP-to-NAP – the 2D NoC allows the sending of data between NAPs within the same column or the same row. In this mode, streams of data are transferred from endpoint to endpoint without further processing.

Peripheral 2D NoC

The peripheral portion of the 2D NoC carries transactions between the FPGA core and the peripheral IP blocks, as well as from NAP-to-NAP when using AXI mode. The 2D NoC can also carry transactions directly between the different peripheral IP blocks. The 2D NoC provides the following services:

- Address decoding
- Transaction command and response routing
- Width adaptation
- Frequency adaptation (clock domain crossing)
- Burst adaptation
- Protocol conversion (e.g., AXI to/from APB)

The peripheral portion of the 2D NoC only carries read and write transactions. It does not carry Ethernet packets or data from the SerDes.

Each row of the 2D NoC presents an AXI initiator to the periphery of the 2D NoC on both the west and east side of the Speedster7t AC7t1500/AC7t1550, and to the west side of the AC7t800. Each column of the 2D NoC presents an AXI responder to the periphery of the 2D NoC on the north side of the FPGA. This structure allows user logic to read or write any external IP or control and status register (CSR) interface and allows any external IP with an initiator interface to access any responder endpoints with attached user logic.

The Speedster7t FPGA 2D NoC has two important features:

- The 2D NoC is usable immediately when reset is released, without configuration of any control and status registers, the FPGA fabric, or the IP interfaces.
- After configuration of IP interfaces and/or control and status registers, the 2D NoC supports transfers between IP cores (such as PCIe and GDDR6) without requiring the FPGA fabric to be configured.

Connectivity Between 2D NoC and Endpoints on FPGA

The connectivity between the 2D NoC and the different endpoints on the FPGA device can be categorized into three scenarios: 2D NoC-to-user logic connectivity, 2D NoC-to-interface IP connectivity, and 2D NoC-to-FCU connectivity.

2D NoC-to-User Logic Connectivity

A 2D NoC access point (NAP) must be instantiated in the user design in order to gain access to the rows and columns of the 2D NoC. There is a 2D NoC column with an initiator NAP and a responder NAP in each cluster. To the FPGA core, these access points look like any other logic columns in the FPGA fabric. The FPGA core provides a clock to the NAP as it does for any other column type. Internally, the NAP has an asynchronous FIFO used to adapt the data rates to what the FPGA can achieve.

2D NoC-to-Interface IP Connectivity

The 2D NoC enables any 2D NoC access point in the FPGA to access any interface IP responder, including any of the GDDR6 AXI interfaces and any of the DDR4/5 or PCIe controllers. It is also feasible to access the control and status interfaces of every IP core, DLL/PLL, and the FCU, through the 2D NoC.

DDR4/5 and GDDR6 Connectivity

Each memory interface presents a 256-bit responder interface to the 2D NoC and accepts read or write transactions. Multiple 2D NoC access points can issue transactions to a single memory interface to utilize the full bandwidth provided by the high-speed memory interfaces.

PCI Express Connectivity

The PCIe IP AXI interface is connected directly to the 2D NoC.

PCIe includes a second interface that does not connect to the 2D NoC, but instead is a direct connection to the FPGA fabric. This interface supports up to 256 Gbps.

2D NoC-to-FCU Connectivity

The FPGA configuration unit (FCU) can issue transactions to the 2D NoC, allowing the configuration logic to set any CSR interface on the device. Initiators on the 2D NoC, such as FPGA logic and the PCIe IP AXI initiator can issue commands to the FCU, allowing for configuration over PCIe and other useful features.

Chapter - 5: Speedster7t FPGA Cryptographic Engine (AC7t800 and AC7t1550 Only)

Overview

The Speedster7t AC7t800 and AC7t1550 FPGAs provide a bi-directional AES-GCM cryptographic engine. A black-box representation of the Speedster7t cryptographic engine must be instantiated in the user design when targeting the Speedster7t AC7t1550 FPGA even if the feature is not used in the design. Only one instantiation of the cryptographic engine is possible and it can only be used with the Speedster7t AC7t1550 FPGA — instantiating this particular engine in the fabric is not supported in any of the other Speedster7t family FPGAs.

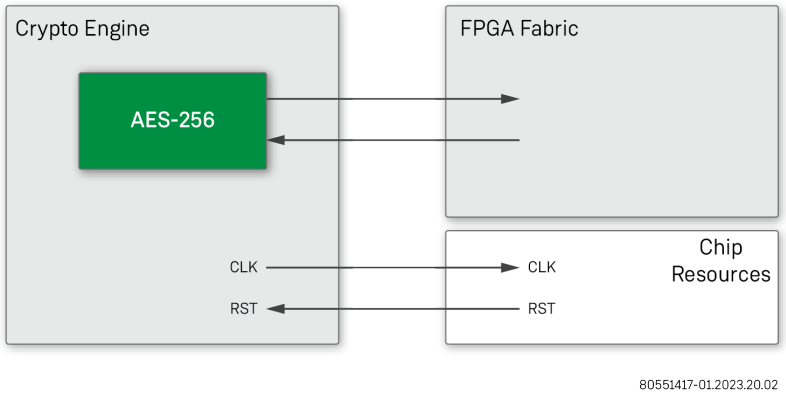


Figure 12: *The Speedster Cryptographic Engine*

The Speedster7t AC7t800 provides the bi-directional AES-GCM cryptographic engine as a dedicated hard block outside of the FPGA fabric core. In this device, the cryptographic engine does not consume any resources in the FPGA fabric, but can be used to encrypt and decrypt data in the FPGA fabric.

AC7t1550 Flow Using the Cryptographic Engine in the FPGA Fabric

The RTL design flow for the cryptographic engine in the Speedster7t AC7t1550 is similar to that of hard IP — the black box representing the cryptographic engine is instantiated in the user RTL. ACE rejects any designs targeting the Speedster7t AC7t1550 which do not instantiate the cryptographic engine.

The cryptographic engine can be accessed via the FPGA fabric and connected to the user RTL design. Synplify Pro is used to synthesize the user RTL into a netlist which ACE uses for floorplanning, placing, routing and generating the final bitstream. The Speedster cryptographic engine is a hard (pre-placed) macro and is resident in the FPGA whether it is used or not.

ACE implements checks to ensure that the cryptographic engine is neither removed nor modified when targeting the AC7t1550. When ACE creates the floor plan for the user design, a bitstream for the user design with the embedded cryptographic engine is generated. The generated bitstream targeting the AC7t1550 is always encrypted using a secret ECDSA authentication key (encoded into ACE) and user-defined AES-256 keys, which must match the secure eFuse keys in the AC7t1550 device. Only bitstreams that use the secret AC7t1550-specific ECDSA authentication key can be loaded into the Speedster7t AC7t1550 FPGAs.

Note

The Speedster7t AC7t1550 supports encrypted bitstreams only.

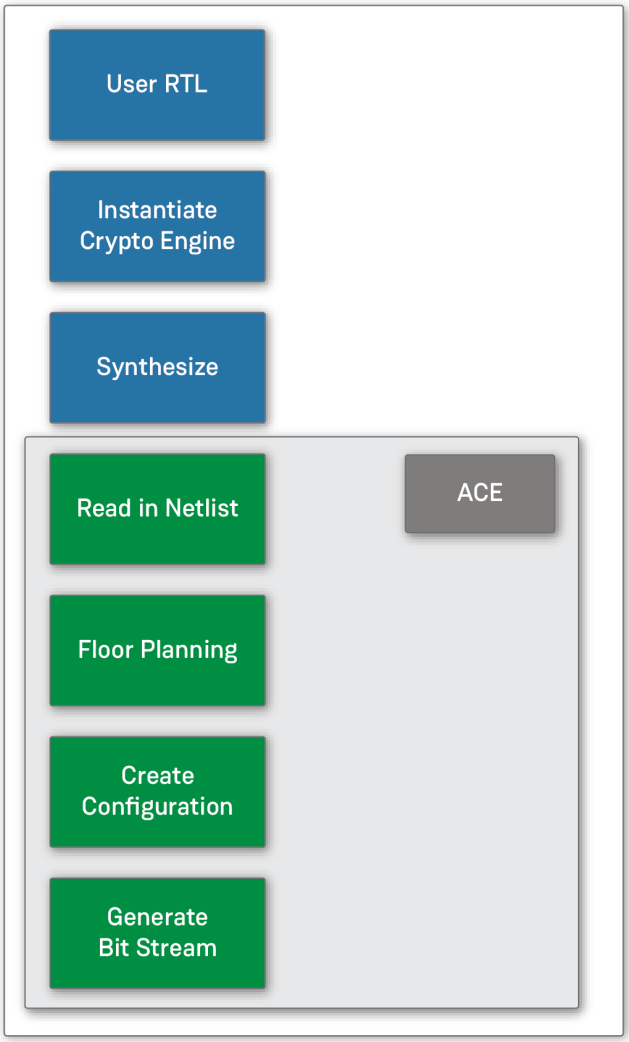


Figure 13: ***Design Flow for the Speedster7t AC7t1500 Cryptographic Engine***

AC7t800 Flow Using the Cryptographic Engine in Dedicated Logic Outside FPGA Fabric

The design flow for the cryptographic engine in the Speedster7t AC7t800 FPGA involves configuring the AES cryptographic engine in the I/O ring. The designer then creates an RTL design connecting the cryptographic engine interface to the FPGA fabric.

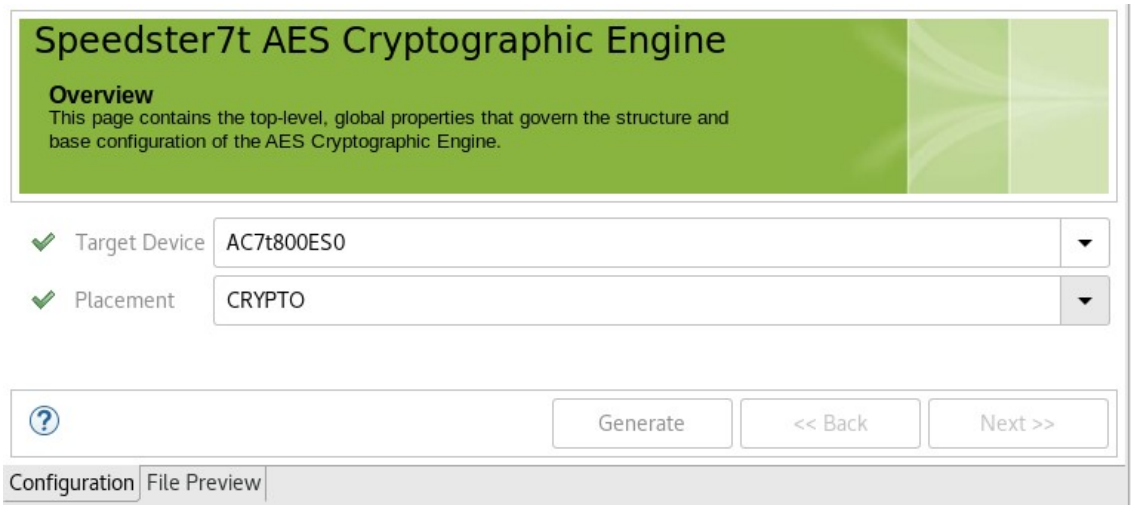


Figure 14: ***Configuration for the Speedster7t AC7t800 Cryptographic Engine***

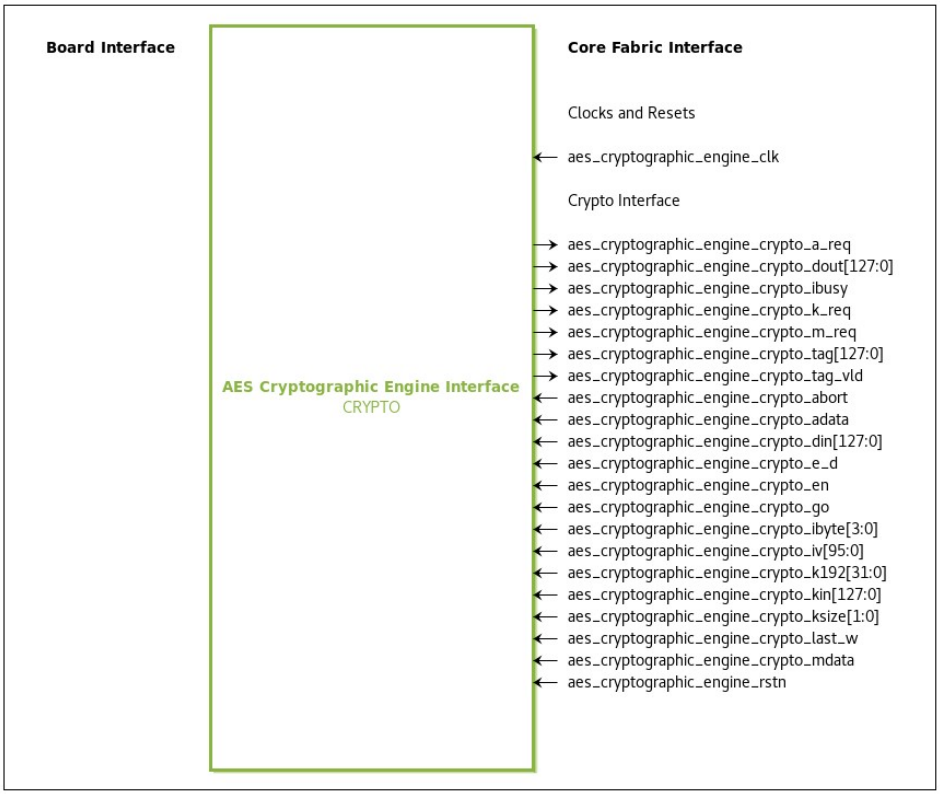


Figure 15: ***Block Diagram for the Speedster7t AC7t800 Cryptographic Engine***

The generated bitstream targeting the Speedster7t AC7t800 FPGA with an AES cryptogrpahic engine can be encrypted using a secret ECDSA authentication key (encoded into ACE) and user-defined AES-256 keys. If the bitstream is encrypted, the keys must match the secure eFuse keys in the AC7t800 FPGA. Only encrypted bitstreams that use the secret AC7t800-specific ECDSA authentication key can be loaded into the Speedster7t AC7t800 FPGAs when using encrypted bitstreams.

Note

The Speedster7t AC7t800 FPGA does not require the use of encrypted bitstreams when using the AES cryptographic engine. The generated bitstream can be encrypted or not, leaving it to the designer to decide.

AES-GCM

By most measures, the advanced encryption standard (AES) has become the *de facto* industry standard for encryption, including adoption by the US federal government. The fully synchronous AES-GCM encryption /decryption engine in the Speedster7t AC7t800 and ACt1550 FPGAs implements Rijndael encoding and decoding in compliance with the NIST AES. Data is processed in 128-bit blocks with a key length of 256.

Key Features

- 25 Gbps at 200 MHz
- Encrypts and decrypts using AES Rijndael block cipher algorithm
- NIST certified
- 96-bit IV length
- Simple, fully synchronous design

Chapter - 6: Speedster7t FPGA Interface Subsystems

Speedster7t FPGAs have dedicated, hard interfaces to support the latest and most advanced versions of serial and memory interfaces used in high-performance networking and compute offload applications including 400G Ethernet, PCI Express Gen5, GDDR6, and DDR4 or DDR5. The combined interfaces achieve up to 8.4 terabits per second of total device bandwidth.

Ethernet

Speedster7t FPGAs include an Ethernet subsystem consisting of 8 SerDes lanes and multiple Ethernet MACs to support a combination of applications. The Ethernet MACs are very flexible and can support multiple ports up to 400G, with each SerDes lane able to achieve a line rate between 10G and 100G. The Ethernet subsystem connects to the FPGA fabric through the two-dimensional network on chip (2D NoC). The following table lists the supported modes.

Table 10: ***Multi-Rate Ethernet Modes Supported per Subsystem***

Mode	Number of Channels	SerDes Rate (Per Lane)	SerDes Lanes
400G	Up to 2	100G	4 lanes per channel.
	1	50G	8 lanes.
200G	Up to 2	50G	4 lanes per channel.
	Up to 4	100G	2 lanes per channel.
100G	Up to 2	25G or 26.5G	4 lanes per channel (KR4 or KP4).
	Up to 4	50G	2 lanes per channel.
50G	Up to 4	25G	2 lanes per channel.
40G	Up to 2	10G	4 lanes per channel.
10G/25G/50G/100G	Up to 8	10G, 25G, 50G, 100G	Independent single-lane applications.

For information on the number of Ethernet subsystems available in a device, refer to the table, Speedster7t Family Overview (see page 10).

Additional Features

- Support for Reed-Solomon FEC (RS-FEC) implementing RS(528, 514) and RS(544, 514) for 100G-KR and 100G-KP applications respectively, as well as 25G and 50G applications
- Support for RS (272, 258) low-latency variant for up to 100G
- Support for 15G (Clause 108) and 50G (Clause 134) and 25/50G Ethernet Consortium specifications
- Configurable Base-R PCS compliant with IEEE 802.3 Clauses 49, 82, 107, 133 for 10G, 25G, 50G operation, respectively
- Independent 64-bit XLGMII MAC interfaces per channel
- Support for error injection to PCS, and received frame error indication
- FEC correctable and un-correctable error reporting
- 1588 l-step for 10G up to 100G, 200G, and 400G
- IEEE 802.3br supported, providing two transmit and receive interfaces for 10G up to 100G
- Optional support for energy efficient Ethernet (EEE) fast-wake (i.e., transfer of LPI sequences, no deep-sleep)
- Optional Base-R (Firecode) FEC according to Clause 74 of IEEE 802.3
- TSN support for 100G and below (IEEE 802.1 Time Sensitive Networking, and IEEE 802.3br Interspersing Express Traffic)
- Interface for register configuration

PCI Express

Speedster7t FPGAs have up to two PCIe interfaces. One interface supports up to 16 lanes (×16). Some Speedster7t FPGAs have a second PCIe interface that supports up to 8 lanes (×8). Both PCIe controller interfaces support operation as either an endpoint or as a root complex. Both PCIe interfaces connect to the FPGA fabric through the two-dimensional network on chip (2D NoC) up to Gen5, and the ×16 interface can also connect to the fabric via the direct-connect interface (DCI) up to 256 Gbps. For information on the number of PCIe subsystems available in a device, refer to the table, Speedster7t Family Overview (see page 10).

Table 11: ***Speedster7t FPGA PCIe Interface Specifications***

Feature	PCIe Port 0	PCIe Port 1
PCI Express Specification	Revision 5.0, Version 0.9	Revision 5.0, Version 0.9
PIPE	Version 5.1.1	Version 5.1.1
Maximum width	×8	×16
Maximum throughput	256 GTs (Gen 5)	512 GTs (Gen 5)
Supported functionality	Root-Port + End-Point	Root-Port + End-Point
DMA support	Yes	Yes
DMA read channels	2	4
DMA write channels	2	4
BAR	6	6
Virtual channels	1	1
Physical functions	2	4
Virtual functions	0	252
Advanced error reporting (AER) support	Yes	Yes
IOV	None	256

GDDR6

Speedster7t FPGAs contain GDDR6 subsystems on the west and east sides to provide external high-bandwidth memory interface support. The controller and PHY implementation are compliant with the JEDEC GDDR6 SGRAM Standard JESD250. See the following table for a summary of the key specs and features.

Each GDDR6 interface operates on two channels, each of which can be enabled independently. The controller supports a wide range of features, including bus utilization optimization, page-hit mitigation, multiport front end (MPFE), reordering and error interrupt.

The GDDR6 subsystems can run up to a data rate of 16 Gbps with device densities from 8 Gb to 16 Gb. The implementation supports GDDR6 up to ×16 in non-clamshell modes and up to ×8 in clamshell modes. For information on the number of GDDR6 subsystems available in a device, see the Speedster7t Family Overview (see page 10) table.

The GDDR6 controllers connect to the other interface subsystems on the Speedster7t FPGAs via the 2D NoC. Additionally, the GDDR6 subsystems can connect directly to the FPGA fabric via an AXI interface with support for full or half-rate clocking. The FPGA fabric and other subsystems can connect to GDDR6 in the following ways:

- A 256-bit AXI interface to the 2D NoC, which can run up to 1 GHz and connects to interface subsystems and FPGA fabric
- A 512-bit AXI direct-to-fabric interface, which can run up to 500 MHz

The PHY ZQ calibration can be configured as Initiator/Responder mode across multiple PHYs.

Furthermore, the IP comes with a memory test and analyzer core to enable standalone testing of the controller and memory during board bring up.

Table 12: *GDDR6 Key Specs and Features on Speedster7t FPGAs*

GDDR6 Feature	Support in Speedster7t AC7t1500/AC7t1550 FPGAs	Support in Speedster7t AC7t800 FPGAs
Memory suppliers	Micron	Micron
Maximum number of memory chips per FPGA	16 (clamshell), 8 (non-clamshell)	16 (clamshell), 8 (non-clamshell)
Maximum total capacity	16GB (1×16 Gb chips in non-clamshell mode per subsystem) 32GB (2×16 Gb chips in clamshell mode per subsystem)	6GB (1×16 Gb chips in non-clamshell mode per subsystem) 12GB (2×16 Gb chips in clamshell mode per subsystem)
Number of channels per GDDR subsystem	2	2
Maximum number of channels total per FPGA	16	6
Width per channel (bits)	16	16
Maximum per-pin data rate supported by FPGA	16 Gbps	16 Gbps
Maximum total bandwidth (No_of_channels_per_FPGA × width_per_channel × rate)	4.0 Tbps	1536 Gbps
Capacity per memory chip	8 Gb–16 Gb	8 Gb–16 Gb
Total memory per FPGA	Up to 16 GB for non-clamshell mode Up to 32 GB for clamshell mode	Up to 6 GB for non-clamshell mode Up to 12 GB for clamshell mode
Memory data rates	12 Gbps, 14 Gbps, 16 Gbps	12 Gbps, 14 Gbps, 16 Gbps

DDR

Speedster7t FPGAs include DDR4/5 interfaces ensuring that memory capacity requirements can be satisfied across a vast application space. The DDR4/5 PHY and controller in Speedster7t FPGAs are compliant to the DDR4/5 JEDEC specification. DDR4 in the Speedster7t AC7t1500/AC7t1550 FPGAs can operate up to 3,200 Mbps in ×4, ×8 and ×16 width configurations. The implementation supports component memories, UDIMM/SO-DIMM form factors as well as RDIMMs and LRDIMMs. DDR5 in the Speedster7t AC7t800 FPGA supports up to 5600Mbps in ×4 and ×8 modes implemented using component DRAMs, UDIMM and RDIMM. Refer to the following tables for a summary of the key specifications and features.

DDR4

Speedster7t AC7t1500/AC7t1550 FPGAs allow for multi-rank support in the DDR4 interface, up to 4 in standard mode, and up to 16 in 3DS mode.

The DDR4 PHY/controller can connect to the other interface subsystems or the FPGA fabric via an AXI interface with support for full, half and quarter-rate clocking. The two connectivity options include:

- A 256-bit AXI interface to the 2D NoC, which can run up to 800 MHz, and connects to interface subsystems and the FPGA fabric.
- A 512-bit AXI direct-to-fabric interface, which can run up to 400 MHz.

Speedster7t FPGAs support AXI compliant low-power interfacing. The DDR4 PHY/controller provides three options for low-power mode:

- A 256-bit AXI interface in low power
- A 512-bit AXI interface in low power
- Memory controller core logic in low power

The option also exists to bypass the entire DDR4 PHY and use these I/O for driving low-performance interfaces such as I^2C, or for optics control, LEDs, etc.

Table 13: ***DDR4 Key Specifications and Features on Speedster7t AC7t1500/AC7t1550 FPGAs***

DDR4 Feature		Support in Speedster7t AC7t1500/AC7t1550 FPGAs.
Memory types		Component, UDIMM, SO-DIMM, RDIMM, LRDIMM.
Memory configurations		×4, ×8, ×16.
Maximum data rate		3200 Mbps.
Burst modes		BL8, burst chop.
Data path widths	Non-ECC	8-bit, 16-bit, 32-bit, 64-bit.
	ECC	32-bit + 7-bit ECC, 64-bit + 8-bit ECC.
Multi-rank support		4 (standard), 16 (3DS).
AXI interface		AXI4 with read reorder buffer and port data widths of 256 and 512 bits.

DDR5

Speedster7t AC7t800 FPGAs have a DDR5 solution implemented as two independent channels, each of which accesses different memories. The Speedster7t AC7t800 FPGA can also be used in DDR4 mode, when only one of the channels is utilized, making the solution similar to the Speedster7t AC7t1500/AC7t1550 FPGAs, and as detailed above.

The DDR5 PHY/controller connects to other interface subsystems or to the FPGA core via the AXI interface. To saturate DDR5 bandwidth, it is required to connect to two AXI ports. The two AXI interface connectivity options include:

- Two 256-bit AXI interfaces to the 2D NoC, which runs up to 700 MHz, and connects to interface subsystems and the FPGA fabric
- A 512-bit AXI direct-to-fabric interface, which can run up to 350 MHz

Optionally, the entire DDR5 PHY may be bypassed and the I/O used for driving low-performance interfaces.

Table 14: ***DDR4 Key Specifications and Features on Speedster7t AC7t800 FPGAs***

DDR5 Feature		Support in Speedster7t AC7t800 FPGAs
Memory types		Component, UDIMM, RDIMM.
Memory configurations		×4, ×8, ×16.
Maximum data rate		5600 Mbps.
Burst modes		BL8, burst chop.
Data path widths	Non-ECC	8-bit, 16-bit, 32-bit, 64-bit.
	ECC	64-bit + 16-bit ECC.
Multi-rank support		4 (standard), 3DS.
AXI interface		AXI4 with read reorder buffer and port data widths of 256 and 512 bits.

Chapter - 7: Speedster7t FPGA Configuration

For normal operation, the Speedster7t FPGA core requires configuration by the end user. Speedster7t FPGAs can be configured via one of four interfaces:

- Flash
- JTAG
- CPU
- PCI Express (PCIe)

A configuration bitstream is generated in ACE by selecting the appropriate configuration interface. The configuration mode of the FPGA is controlled via mode select pins on the configuration interface of the FPGA. These pins can be driven via hardware on the board or by another device such as a CPLD. The option exists to generate an encrypted and authenticated bitstream. If this feature is used, the Speedster7t FPGA first secures the hardware and then authenticates and decrypts the bitstream before programming the FPGA fabric.

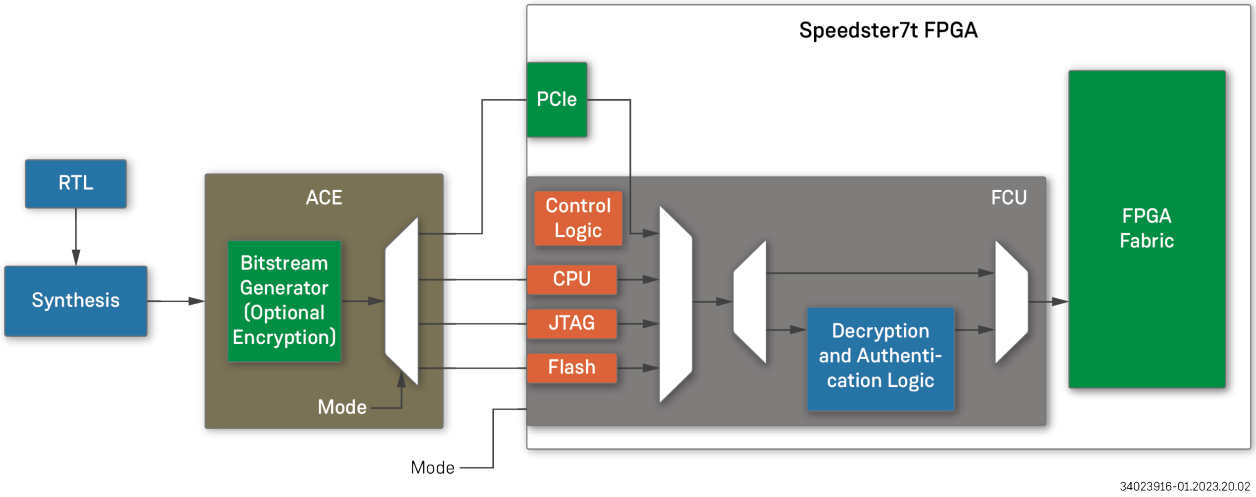


Figure 16: ***Bitstream Generation and Configuration Process***

Flash Mode

The serial flash programming mode allows flash memories to be used to configure the Speedster7t FPGA. In this mode, the Speedster7t FPGA is the controller, and therefore, supplies the clock to the flash memory. Flash programming supports SPI (single-bit interface to the flash memory), dual (two-bit interface to the flash memory), quad (four-bit interface to the flash memory) and octa (eight-bit interface to the flash memory) modes. Additionally, the Speedster7t FPGA can interface to one device (1D) or four devices (4D) of flash memory modules on the board. The bitstream size is entirely dependent on the size of the fabric. It is important that the flash solution chosen is large enough to store the bitstream data.

Flash mode also supports the remote update with fallback option feature, wherein two bitstreams can be simultaneously stored in the flash device and either one chosen to program the FPGA. The update can be triggered remotely via a user application that writes to appropriate registers on the Speedster7t device. If bitstream programming fails for some reason, the fallback logic loads a known good bitstream which allows the device to resume normal operation.

JTAG Mode

The Speedster7t FPGA JTAG Tap controller is IEEE Std 1149.1 and 1149.6 (AC JTAG) compliant. The JTAG interface also provides debug capability for the Achronix on-chip logic analyzer tool, Snapshot, and other debug tools. The Speedster7t FPGA can be configured as a single JTAG device, or as part of a series of cores within a system connected on the JTAG chain.

CPU Mode

In CPU mode, an external CPU acts as the controller for programming operations. This mode offers a high-speed method for loading configuration data. CPU mode uses either a 1-, 8-, 16-, or 32-bit wide parallel interface. A 128-bit wide parallel interface is available, but with limitations. The 128-bit mode does not support encrypted bitstreams, and can only be used when the DDR interface is disabled, as it shares pins with the DDR interface. This mode provides for the widest data interface and a maximum supported clock rate of 250 MHz.

Note

If interested in using 128-bit mode, please contact Achronix for support.

PCIe Mode

PCIe mode requires two-stage programming. First, the I/O ring portion of the Speedster7t device is configured via flash, JTAG, or CPU. When the PCIe interface is enabled, bitstream programming is performed via indirect addressing, where the AXI responder interface in the Speedster7t FPGA receives the bitstream in the form of a PCIe packet and writes that data to the programming registers.

Bitstream Security Features

Achronix recognizes the importance of protecting the sensitive IP placed onto the FPGA. To provide a high level of protection, Speedster7t FPGAs have a number of features to support bitstream encryption as well as authentication. These features ensure that the design configuration on the FPGA cannot be accessed and also ensures that the design is the one intended. Speedster7t FPGAs provide this high level of security through the following features:

- Support for ECDSA authenticated and AES-GCM encrypted bitstream
- Dynamic power analysis (DPA) protection to prevent side-channel attacks
- Physically unclonable function (PUF) for tamper-proof protection
- Securely stores both public and encrypted private keys

With this security solution deployed, customer designs are secure. Even with possession of the device, the underlying design cannot be extracted, cannot be reverse engineered, nor can the design be altered in any way.

Chapter - 8: Snapshot

Snapshot is the real-time design debugging tool for Achronix FPGAs and eFPGA cores. The Snapshot debugger, which is embedded in ACE software, delivers a practical platform to observe the signals of a user design in real-time. To use the Snapshot debugger, the Snapshot macro must be instantiated inside the user RTL. After instantiating the macro and programming the FPGA, the design may be observed through the Snapshot debugger GUI within ACE, or via the `run_snapshot` Tcl command API.

The Snapshot macro can be connected to any logic signal mapped to the Achronix core, to monitor and potentially trigger on that signal. Monitored signal data is collected in real time in regular BRAMs prior to being transferred to the ACE Snapshot GUI. The Snapshot macro has configurable monitor width and depth, as well as other configuration parameters, allowing control over resource usage.

The ACE Snapshot GUI interacts with the hardware via the JTAG interface. Interactively-specified trigger conditions are transferred to the design, and collected monitor data is transferred back to the GUI, which displays the data using a built-in waveform viewer. The following figure shows the components involved in a Snapshot debug session:

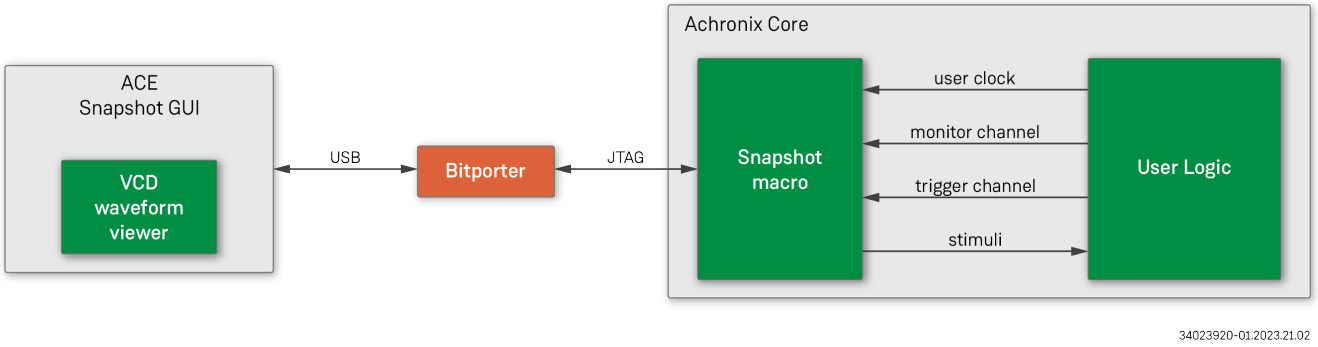


Figure 17: *Snapshot Overview*

Features

The Snapshot macro samples user signals in real time, storing the captured data in one or more BRAMs. The captured data is then communicated through the JTAG interface to the ACE Snapshot GUI. The implementation supports the following features:

- Monitor channel capture width of 1 to 4064 bits of data.
- Monitor channel capture depth of 512 to 16384 samples of data at the user clock frequency.
- Trigger channel width of 1 to 40 bits.
- Supports up to three separate sequential trigger conditions. Each trigger condition allows for the selection of a subset of the trigger channel, with AND or OR functionality.
- Bit-wise support for edge-sensitive (rise/fall) or level-sensitive triggers.
- The ACE Snapshot GUI allows the specification of trigger conditions and circuit stimuli at runtime.
- An optional initial trigger condition, specified in RTL parameters, to allow capture of data immediately after startup, before interaction with the ACE Snapshot GUI.
- A stimuli interface, 0 to 512 bits wide, that allows the driving values into the Achronix core logic from Snapshot. Stimuli values are specified with the ACE Snapshot GUI and made available before data capture.
- Optionally, the data capture can include values prior to the trigger event. This "pre-store" amount can be specified in increments of 25% of the depth.
- Captured data is saved in a standard VCD waveform file. The ACE Snapshot GUI includes a waveform viewer for immediate feedback.
- The VCD waveform file includes a timestamp for when the Snapshot was taken.
- ACE automatically extracts the names of the monitored signals from the netlist, for easy interpretation of the waveform.
- A repetitive trigger mode, in which repeated Snapshots are taken and collected in the same VCD file.
- The JTAG interface can be shared with the user design.
- A Tcl batch/script mode interface is provided via the `run_snapshot` Tcl command.

Chapter - 9: Speedster7t FPGA Timing Data

Speed Grades

The core voltage for Speedster7t FPGAs varies by device speed grade (refer to the table, Speedster7t Speed Grades (see page 64)).

Speedster7t AC7t1500/AC7t1550 C1, C2, and C3L (Extended Commercial Temperature Range: 0°C to +100°C)

I/O Ring

SerDes (Ethernet Mode)

The SerDes data/clock signals at parallel ports are routed directly to the Ethernet/PCS controller.

Table 15: *SerDes Maximum Clock Rates (Ethernet Mode)*

Clock	Speed Grade			Units	Description
	3L	2	1		
tx_block_clk	830			MHz	SerDes transmit clock at the parallel ports.
rx_block_clk	830			MHz	SerDes receive clock at the parallel ports.

Table 16: *SerDes Line Rates (Ethernet Mode)*

Width at Parallel Ports	Speed Grade			Units
	3L	2	1	
128 bits	106.25			Gbps
64 bits	53.125			Gbps
32 bits	26.56			Gbps
16 bits	13.28			Gbps

For the full list of line rates supported with Ethernet, refer to the *Speedster7t Ethernet User Guide* (UG097).

SerDes (PCIe Mode)

The SerDes data/clock signals at parallel ports are routed directly to the PCIe controller.

Table 17: *SerDes Maximum Clock Rates (PCIe Mode)*

Clock	Speed Grade			Units	Description
	3L	2	1		
tx_block_clk	500	1000	1000	MHz	SerDes transmit clock at the parallel ports.
rx_block_clk	500	1000	1000	MHz	SerDes receive clock at the parallel ports.

See the following for maximum PCIe data rates (see page 52).

SerDes (PCS with PCIe PIPE)

The SerDes data/clock signals at parallel ports are routed to the PCS with PCIe PIPE to enable soft controllers in the fabric, up to Gen4.

Table 18: *SerDes Maximum Clock Rates (PCS with PCIe PIPE)*

Clock	Speed Grade			Units	Description
	3L	2	1		
tx_block_clk	500			MHz	SerDes transmit clock at the parallel ports.
rx_block_clk>	500			MHz	SerDes receive clock at the parallel ports.

For more details on using the PCS with PCIe PIPE, refer to the *Speedster7t SerDes User Guide* (UG099).

SerDes (PCS with Gearbox)

The SerDes data/clock signals at parallel ports are routed to the PCS with Gearbox (66b/64b and 67b/64b supported).

Table 19: *SerDes Maximum Clock Rates (PCS with Gearbox)*

Clock	Speed Grade			Units	Description
	3L	2	1		
tx_block_clk	402.83			MHz	SerDes transmit clock at the parallel ports.
rx_block_clk	402.83			MHz	SerDes receive clock at the parallel ports.

Table 20: *SerDes Line Rates (PCS with Gearbox)*

Width at Parallel Ports	Speed Grade			Units
	3L	2	1	
64 bits	25.78125			Gbps

For more details on using the PCS with Gearbox, refer to the *Speedster7t SerDes User Guide* (UG099).

SerDes (Raw Mode)

The SerDes data/clock signals at parallel ports bypass the Ethernet/PCIe/PCS controller and go directly to the fabric core.

Table 21: *SerDes Maximum Clock Rates (Raw Mode)*

Clock	Speed Grade			Units	Description
	3L	2	1		
tx_block_clk	400	500	550	MHz	SerDes TX clock at the parallel ports.
rx_block_clk	400	500	550	MHz	SerDes RX clock at the parallel ports.

Table 22: *SerDes Line Rates (Raw Mode)*

Width at Parallel Ports	Speed Grade			Units
	3L	2	1	
128 bits	50	53.125 (1)	53.125 (1)	Gbps
64 bits	20.625	26.5625 (1)	26.5625 (1)	Gbps
40 bits	16	20	20.625 (1)	Gbps
32 bits	10.3125 (1)	10.3125 (1)	10.3125 (1)	Gbps
20 bits	–	–	10.3125	Gbps
16 bits	–	–	10.3125	Gbps

Table Notes

1. The data rate is limited by the highest achievable parallel clock frequency for raw mode (see the previous table), and the data rates supported by Ethernet.

For more details on using the raw SerDes that bypasses the PCS and connects the PMA directly to the fabric core, refer to the *Speedster7t SerDes User Guide* (UG099).

Ethernet

Table 23: *Ethernet Maximum Clock Rates*

Clock	Speed Grade			Units	Description
	3L	2	1		
ref_clk	900			MHz	Ethernet reference clock.
ff_clk	782			MHz	Ethernet FIFO clock.

Table 24: *Ethernet Line Rates*

Width at Parallel Ports	Speed Grade			Units
	3L	2	1	
64 bits	53.125			Gbps
128 bits	106.25			Gbps

DDR4

Table 25: *DDR4 Line Rate*

Width at Parallel Ports	Rank	Speed Grade			Units
		3L	2	1	
64 bits (per data pin)	1	2666	2666	3200	Mbps
64 bits (per data pin)	2	2133	2400	2400	Mbps
64 bits (per data pin)	4	1333	1600	1600	Mbps

GDDR6

Table 26: *GDDR6 Line Rate*

Width at Parallel Ports	Speed Grades			Units
	3L	2	1	
32 bits (per data pin)	14	14	16	Gbps

PCIe ×8 (PCIE_0)

Table 27: *PCIe ×8 Maximum Data Rates*

Speed Grade			Units	Description
3L	2	1		
16 (Gen4)	32 (Gen5)	32 (Gen5)	GT/s	Access FPGA via 2D NoC.

Table 28: *PCIe ×8 Other Specifications*

Item	Value	Units
Number of lanes supported	×1, ×4, ×8	–

PCIe x16 (PCIE_1)

Table 29: *PCIe ×16 Maximum Data Rates*

Speed Grade			Units	Description
3L	2	1		
16 (Gen4)	32 (Gen5)	32 (Gen5)	GT/s	Access FPGA via 2D NoC.
16 (Gen4)	16 (Gen4)	16 (Gen4)	GT/s	Access FPGA via DCI AXI.

Table 30: *PCIe ×16 Other Specifications*

Item	Value	Units
Number of lanes supported	×1, ×4, ×8, ×16	–

Fabric and Macros

PLL

Table 31: *PLL Specifications*

Speed Grade			Units	Description
3L	2	1		
600			MHz	Maximum reference input clock frequency.
5			MHz	Minimum reference input clock frequency.
1			ns	Minimum pulse width high/low.
50			%	Input duty cycle.
1			µs	Minimum reset pulse width.
8000			MHz	Maximum VCO frequency.
4000			MHz	Minimum VCO frequency.
±2			%	PLL output jitter.
35			µs	Maximum PLL lock time.
2040			MHz	Maximum PLL output clock frequency.
7.5			MHz	Minimum PLL output clock frequency.

DLL

Table 32: *DLL Specifications*

Speed Grade			Units	Description
3L	2	1		
300			MHz	Minimum reference input clock frequency.
1333			MHz	Maximum reference input clock frequency.
50			Reference clock cyles	Maximum DLL lock time.
1			µs	Minimum reset pulse width.

BRAM

Table 33: *BRAM Specifications*

Speed Grade			Units	Description
3L	2	1		
622	750	802	MHz	BRAM_FIFO without ECC (IP to Output Reg).
498	600	642	MHz	BRAM_FIFO_with ECC (IP to Output Reg).
622	750	802	MHz	BRAM_SDP without ECC (IP to Output Reg).
498	600	642	MHz	BRAM_SDP with ECC (IP to Output Reg).
584	485	453	ps	Input Setup without ECC (address and data).
706	586	548	ps	Input Setup with ECC (address and data).
837	695	650	ps	Input Setup for control (we, ce, etc.)
1655	1374	1284	ps	Output C→Q without ECC (from IP).
1995	1656	1548	ps	Output C→Q with ECC (from IP).
670	556	520	ps	Output C→Q (from Output Reg).

LRAM

Table 34: *LRAM Specifications*

Speed Grade			Units	Description
3L	2	1		
498	600	642	MHz	LRAM_FIFO (IP to Output Reg).
622	750	802	MHz	LRAM_SDP (IP to Output Reg)
735	610	570	ps	Input Setup for address and data.
1100	913	853	ps	Input Setup for control (rst, wren, rden).
583	484	452	ps	Output C→Q (from Output Reg).
1054	875	818	ps	Read Address to Data Out (Un-clocked).

MLP

Table 35: *MLP Specifications*

Speed Grade			Units	Description
3L	2	1		
622	750	802	MHz	Integer mult-add frequency (3 cycle latency).
622	750	802	MHz	Integer parallel mult frequency (2 cycle latency).
622	750	802	MHz	Floating point mult-add frequency (6 cycle latency).
622	750	802	MHz	Floating point mult frequency (4 cycle latency).

2D NoC

Table 36: *2D NoC Specifications*

Speed Grade			Units	Description
3L	2	1		
200			MHz	Maximum 2D NoC input reference clock.
1400 (1)	1700	2000	MHz	Maximum 2D NoC operating frequency.

Table Notes

1. Maximum operating frequency when using 400GE: up to 2050 MHz.

GPIO

Table 37: *GPIO Specifications*

Speed Grade			Units	Description
3L	2	1		
500			MHz	Maximum Output Frequency.

CLKIO

Table 38: *CLKIO Specifications*

Speed Grade			Units	Description
3L	2	1		
1000 (1)			MHz	CLKIO REFIO Max Input Frequency.
1000			MHz	CLKIO REFIO Max Output Frequency.
500			MHz	CLKIO MSIO Max Input Frequency.
500			MHz	CLKIO MSIO Max Output Frequency.

Table Notes

1. CLKIO REFIO Max Input Frequency of 1000 MHz is possible if using PLL in bypass mode. If using as a reference input to a PLL, maximum input frequency is 600 MHz.

Chapter - 10: Speedster7t AC7t1500/AC7t1550 2597-Pin FBGA

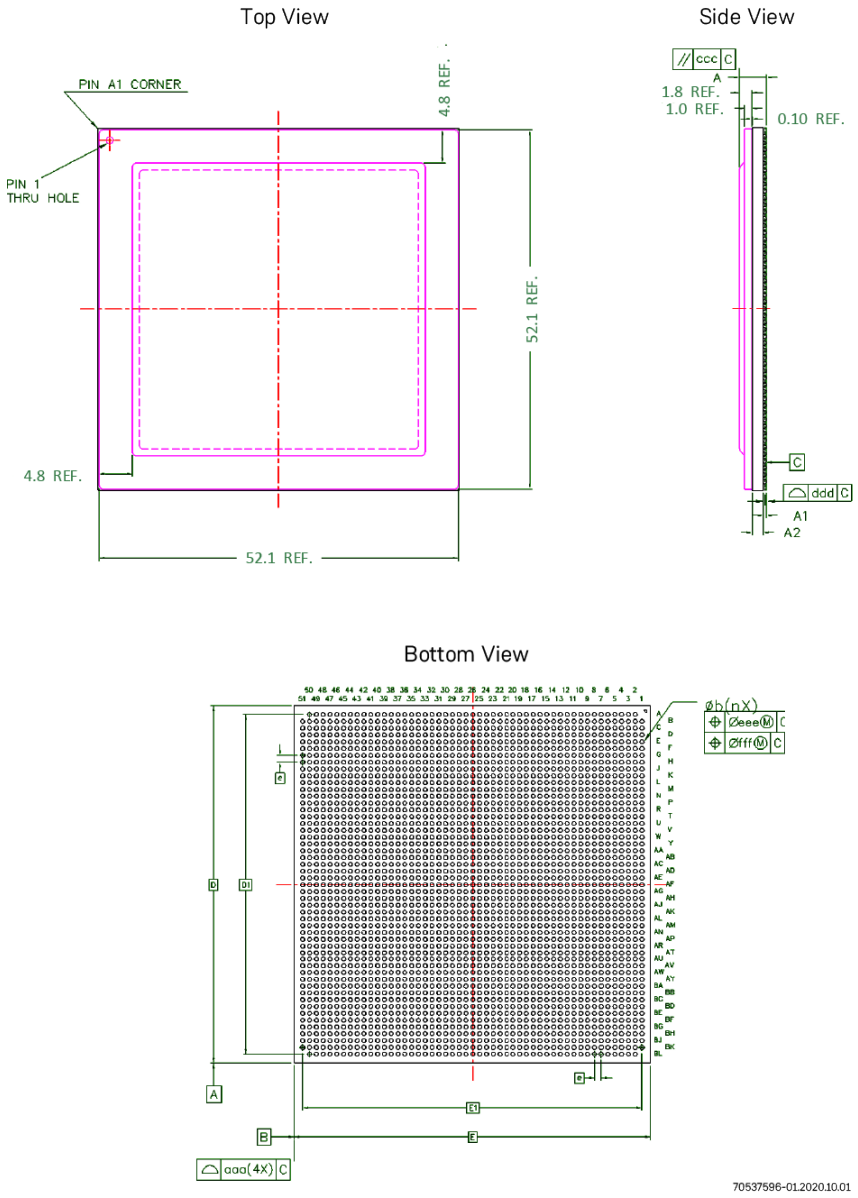


Figure 18: ***2597-Pin FBGA Package***

Table 39: *2597-Pin FBGA Package Dimensions*

Parameter	Symbol	Common Dimensions		
		Min	Nom	Max
TOTAL THICKNESS	A	3.757	3.952	4.147
STAND OFF	A1	0.400	–	0.600
SUBSTRATE THICKNESS	A2	1.552 REF		
BODY SIZE	E	52.5 BSC		
	D			
BALL DIAMETER		0.600		
BALL WIDTH	b	0.500	–	0.700
BALL PITCH	e	1.00 BSC		
BALL COUNT	n	2597		
EDGE BALL CENTER TO CENTER	E1	50 BSC		
	D1			
PACKAGE EDGE TOLERANCE	aaa	0.200		
TOP PARALLELISM	CCC	0.350		
CO PLANARITY	ddd	0.200		
BALL OFFSET (PACKAGE)	eee	0.250		
BALL OFFSET (BALL)	fff	0.300		

Chapter - 11: Speedster7t I/O Electrical Specification

This section provides a brief summary of the target electrical specification of the MSIO and REFIO. The MSIO can be found in the GPIO as well as MSIO portions of the CLKIO interface. The REFIO signals are only a part of the CLKIO. The relevant electrical specifications from the associated standards document are used for compliance testing.

Speedster7t AC7t1500/AC7t1550 Absolute Maximum Ratings

The following table lists absolute maximum ratings, beyond which damage to the device may occur.

Table 40: *Absolute Maximum Ratings*

Parameter Symbol	Min	Typ	Max	Unit	Description
VDDIO	1.07	1.1	1.14	V	Analog supply for CLKIO (`CLKIO_*_VDDIO`) and GPIO (`GPIO_*_VDDIO`): CLKIO bank voltages: 1.8V, 1.5V GPIO bank voltages: 1.8V, 1.5V, 1.35V, 1.2V, 1.1V
	1.16	1.2	1.24	V	
	1.31	1.35	1.4	V	
	1.45	1.5	1.55	V	
	1.75	1.8	1.86	V	
VREF	0.53	0.55	0.57	V	Reference voltage supply for CLKIO (`CLKIO_*_VREF`) and GPIO (`GPIO_*_VREF`).
	0.58	0.6	0.62	V	
	0.65	0.675	0.7	V	
	0.73	0.75	0.78	V	
	0.87	0.9	0.93	V	
T_J	-40	25	100	°C	Junction operating temperature.

Speedster7t AC7t1500/AC7t1550 MSIO Electrical Specification

The following table lists the target electrical specification for all MSIO in the Speedster7t AC7t1500/AC7t1550 FPGAs. The MSIO are used as GPIO and the MSIO section of CLKIO.

Table 41: *MSIO Electrical Specification*

Parameter Symbol	Min	Typ	Max	Unit	Description
C_{IN}			5	pF	Input capacitance.
I_L			30	uA	Input/Output leakage.
I_{L_VREF}			5	uA	Vref pad leakage.
I_{PU}	30		150	uA	Pad pull-up (when enabled), V_{in} = 0 V.
I_{PD}	30		150	uA	Pad pull-down (when enabled), V_{in} = VDDIO.
ODT_{CAL}	-10%		10%		Calibrated ODT accuracy (MSIO_ZCAL in same bank).
ODT_{CAL_DIFF}	-20%		20%		Calibrated differential ODT accuracy (MSIO_ZCAL in same bank).
V_{INL}	-200		VREF-90	mV	Input logic low level.
V_{INH}	VREF+90		VDDIO+200	mV	Input logic high level.
F_{MAX}			500	MHz	Maximum I/O frequency (Dependent on-board level loading and SI).
I_{DRV}	2		16	mA	1.8V LVCMOS drive levels.
V_{ST}	30	40	60	mV	Schmitt trigger hysteresis.
V_{REF}	0.3 *VDDIO		0.7 *VDDIO	V	Supported VREF levels.
SR_{HSUL}	2			V /ns	Slew rate for HSUL configuration with C_{load} = 5pF, R_{out} = 50Ω and VDDIO = 1.8 V.
SR_{HSTL}	0.83			V /ns	Slew rate for HSTL configuration with C_{load} = 20pF, R_{out} = 50Ω and VDDIO = 1.8 V.
SR_{SSTL}	0.6			V /ns	Slew rate for SSTL configuration with C_{load} = 30pF, R_{out} = 50Ω and VDDIO = 1.8 V
SR_{LVCMOS}	3			V /ns	Slew rate for LVCMOS configuration with C_{load} = 5pFand VDDIO = 1.8V.

Speedster7t AC7t1500/AC7t1550 REFIO Electrical Specification

The following table lists the target electrical specification for all REFIO in the Speedster7t AC7t1500/AC7t1550 FPGAs. The REFIO are used in the CLKIO.

Table 42: *REFIO Electrical Specification*

Parameter Symbol	Min	Typ	Max	Unit	Description
C_{IN}			5	pF	Input capacitance.
I_L			30	uA	Input/Output leakage.
ODT_{CAL_DIFF}	-15%		15%		Calibrated differential ODT accuracy (MSIO_ZCAL in same bank).
$V_{IN\_DIFF\_PEAK}$	100	350	800	mV	Input levels in differential RX mode.
V_{CM_DC}	0.3	1.2	1.425	V	Board level DC coupling receive common mode.
V_{CM_AC}	0.6		1.1	V	Board level AC coupling receive common mode.
$Jitter_{intrinsic}$			0.3	ps rms 12kHz-75MHz	Intrinsic receive buffer jitter for 150MHz reference clock with 200mV differential peak swing and 400ps rise/fall time (slew rate of 1V/ns).
F_{MAX}			1000	MHz	Maximum I/O frequency (dependent on-board level loading and SI).
F_{MIN}	10			MHz	Minimum I/O frequency (dependent on-board level loading and SI).
I_{DRV}	2		16	mA	1.8V LVCMOS drive levels.

Chapter - 12: Speedster7t FPGA Power Rails, Speed Grades and Ordering Information

Speedster7t Power Supplies

Table 43: ***Speedster7t Power Supply Requirements by Pin Name***

Min Voltage (V)	Typ Voltage (V)	Max Voltage (V)	AC Ripple (mV pk-pk)	Description
VCC				
0.84	0.85	0.86	17	Digital supply for the interface IP and 2D NoC in the fabric.
TS_VDDA				
1.78	1.8	1.82	36	Analog power supply to the temperature sensor.
CLKIO_<NE/NW/SE/SW>_VDDIO				
1.46	1.5	1.61	30	Analog supply for clock I/O.
1.75	1.8	1.93	30	
CLKIO_<NE/NW/SE/SW>_VREF.				
0.73	0.75	0.8	15	Reference voltage supply for the CLKIO.
0.87	0.9	0.96	15	
CORE_VDD				
Speed grade 1 – 0.90V				Power supply for the FPGA fabric based on the selected speed grade.
0.89	0.90	0.91	36	
Speed grade 2 – 0.85V				
0.84	0.85	0.86	34	
Speed grade 3L – 0.75V				
0.74	0.75	0.76	30	
DDR4_S0_VAA				
1.78	1.8	1.82	36	Analog supply for the DDR PLL.
DDR4_S0_VDDQ				
1.16	1.2	1.24	38	I/O domain power supply for the DDR4 PHY.

Min Voltage (V)	Typ Voltage (V)	Max Voltage (V)	AC Ripple (mV pk-pk)	Description
ENOC_<N/NE/NW/S/SE/SW>_PLL_VDDA				
1.78	1.8	1.82	36	Analog supply for the peripheral ring of the 2D NoC PLLs.
FUSE_VDD2				
1.78	1.8	1.82	36	Analog supply for the eFUSE module.
FCU_VDDIO				
1.78	1.8	1.82	36	Analog supply for the GPIO associated with FCU/JTAG.
GCG_<NE/NW/SE/SW>_PLL_VDDA				
1.78	1.8	1.82	36	Analog supply for the clock generator PLLs.
GDDR6_<E/W>_VDDR				
0.83	0.85	0.88	34	Digital supply for GDDR6 PHY. This supply is used for level shifting input signals from VDDR to VDDA domain and all output signals from VDDA to VDDR domain.
GDDR6_<E/W>_VDDA				
0.83	0.85	0.87	26	Analog power supply for GDDR6 PHY. This supply is used for digital logic, custom digital, data pipes and receive delay lines. Also used as analog circuit supply, clocking, global and local clock trees.
GDDR6_<E/W>_VDDIO				
1.32	1.35	1.38	27	GDDR6 I/O power supply.
GDDR6_<E/W>_VDDP				
1.32	1.35	1.38	27	PLL supply for GDDR6 PHY.
SRDS_N_PA_VDDH				
1.16	1.2	1.3	10	SerDes analog high-power supply.
SRDS_N_PA_VDDL				
0.73	0.75	0.81	10	SerDes analog low-power supply.
GPIO_<N0/S0>_VDDIO				
1.07	1.1	1.14	30	Analog supply for the GPIO.
1.16	1.2	1.24	40	
1.31	1.35	1.4	50	
1.45	1.5	1.55	60	
1.75	1.8	1.86	100	

Min Voltage (V)	Typ Voltage (V)	Max Voltage (V)	AC Ripple (mV pk-pk)	Description
GPIO_<N0/S0>_VREF				
0.53	0.55	0.57	15	Reference voltage supply for the GPIO.
0.58	0.6	0.62	20	
0.65	0.675	0.7	25	
0.73	0.75	0.78	30	
0.87	0.9	0.93	50	

Speedster7t Speed Grades

Table 44: *Speedster7t Speed Grades*

Speed Grade	Nominal Voltage (V)	2D NoC	Ethernet	GDDR6	PCIe	DDR4	SerDes (DCI)
1	0.90	2 GHz	400 Gbps	16 Gbps	Gen5	3,200 Mbps	550 MHz
2	0.85	1.7 GHz	400 Gbps (1)	14 Gbps	Gen5	2,666 Mbps	500 MHz
3L	0.75	1.4 GHz	400 Gbps (1)	14 Gbps	Gen4	2,666 Mbps	400 MHz

Table Notes

1. Operation at 400G is supported only when the design routes Ethernet traffic across two separate 2D NoC columns.

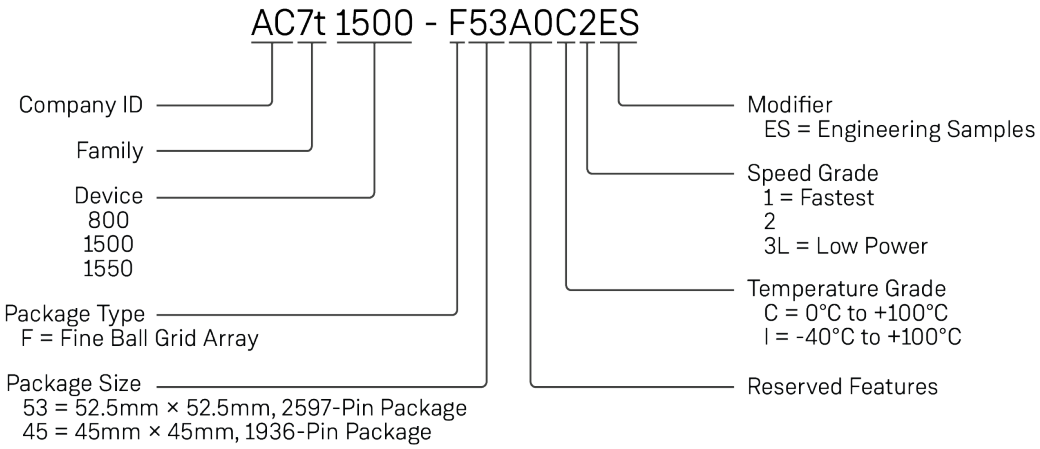
Speedster7t Lifetime and Temperature Ranges

Achronix Speedster7t FPGAs have an operating lifetime of ten years and can support the following temperature grades (junction temperature listed):

- Extended Commercial (0°C to +100°C)
- Industrial (−40°C to +100°C)

> **Note**
>
> For details on Extended and Industrial temperature ranges, contact support@achronix.com.

Speedster7t Ordering Codes



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Revision History

Version	Date	Description
1.0	24 Mar 2020	• Initial Achronix release.

1.1	12 Jun 2020	• Updated number of special-purpose I/O (SPIO) in table, Speedster7t FPGA Family Features Table (see page 10).
		• Added new sections:
		  • Special-Purpose I/O (SPIO) (see page 24)
		  • Speedster7t FPGA Timing Data (see page 48)

1.2	07 Aug 2020	• Added new sections for Fabric and Macro in the chapter, Speedster7t FPGA Timing Data. (see page 48)
1.3	02 Oct 2020	• Added the chapter, Speedster7t Packaging Information (see page 57) with details on the 2597-pin FBGA.
1.4	18 Mar 2021	• Added support for the Speedster7t AC7t1550 FPGA. • Added the chapter, Speedster7t FPGA Cryptographic Engine (AC7t800 and AC7t1550 Only) (see page 34).
1.5	29 Jun 2021	• Updated Speedster7t Product Family table, and ordering codes. • Replaced all instances of "NoC" replaced with "2D NoC" and made minor edits.
1.6	21 Jan 2022	• Corrected maximum number of memory chips for GDDR6 in the chapter Speedster7t FPGA Interface Subsystems (see page 38). • Minor clarifications and updates.
1.7	26 Jul 2022	• Corrected maximum total memory capacity for GDDR6 memory in clamshell mode in the chapter Speedster7t FPGA Interface Subsystems (see page 38 38). • Added section Speedster7t I/O Electrical Specification (see page 59). • Updated with more details for Speedster7t AC7t800 FPGAs.
1.8	17 May 2023	• Updates to Speedster7t Speed Grade table, temperature ranges, and ordering code figure in the chapter Speedster7t FPGA Power Rails, Speed Grades and Ordering Information (see page 62). • Updates to timing data in the chapter Speedster7t FPGA Timing Data (see page 48). • Updates to Speedster7t FPGA Cryptographic Engine (AC7t800 and AC7t1550 Only) (see page 34) for Speedster7t AC7t800.

Version	Date	Description
		• Added section on Fabric Clusters in Speedster7t Fabric Architecture (see page 13). • Updates to Speedster7t AC7t1550 resources in Speedster7t FPGA Family Features Table (see page 10).