Speedster7t FPGA Datasheet (DS015)

Speedster FPGAs

Preliminary Data

Achronix®
Data Acceleration

Copyrights, Trademarks and Disclaimers

Preliminary Data

This document contains preliminary information and is subject to change without notice. Information provided herein is based on internal engineering specifications and/or initial characterization data.

Achronix Semiconductor Corporation

2903 Bunker Hill Lane
Santa Clara, CA 95054
USA

Website: www.achronix.com
E-mail : info@achronix.com

Table of Contents

Chapter - 1: Overview

Introducing the Speedster7t FPGA Family

Achronix's new, high-performance, 7nm Speedster®7t FPGA family is specifically designed to support extremely high bandwidth requirements for demanding applications including data-center workloads and networking infrastructure. The processing tasks associated with these high-performance applications, specifically those associated with artificial intelligence and machine learning (AI/ML) and high-speed networking, represent some of the most demanding processing workloads in the data center.

Several performance criteria characterize these data-center and networking workloads:

- The ability to handle high-speed data rates from a host processor's PCIe port and up to 400 Gbps Ethernet ports.
- The ability to store multiple gigabytes of incoming data and to access that data quickly for processing within the FPGA.
- The ability to move massive amounts of data among the FPGA's I/O ports, its internal memory, attached external memory, and its on-chip computing resources.
- The ability to process high computational loads with tera-operations-per-second of performance.

The Speedster7t FPGA family can more than satisfy each of these performance criteria with appropriately scaled and optimized on-chip resources.

Handling High-Speed, Incoming and Outgoing Data

For data-center and networking applications, high-speed data enters an FPGA-based processing node in two fundamental ways: through PCIe connections to a host processor and via high-speed Ethernet connections to other data-center resources. The Speedster7t family is designed to maximize data rates over these connections by implementing a number of PCIe Gen5 interfaces for the host-processor connection(s) and multiple SerDes ports capable of supporting 400 Gbps Ethernet connections. Both of these I/O standards represent the fastest, most recent specifications for inter- and intra-system data communications used in data centers and myriad other FPGA-based applications. The Speedster7t FPGA's multiple, high-speed I/O ports support data rates that data centers expect to see in the near future.

Fast, High-Capacity Memory Storage

Most FPGAs store data that must be accessed quickly in on-chip SRAM. The Speedster7t FPGA family is no exception, incorporating a substantial amount of memory. However, the sheer volume of data that must be handled by many data-center applications almost universally overwhelms any available amount of on-chip SRAM, even when the FPGA in question is fabricated with 7nm FinFET process technology.

Consequently, the Speedster7t is designed with multiple GDDR6 graphics SDRAM ports. In the immediate future, GDDR6 SDRAMs will provide the fastest SDRAM access speeds with the lowest DRAM cost (per stored bit), at power levels equivalent to LPDDR5 SDRAM. Together, these characteristics make GDDR6 SDRAM interfaces the best choice for next-generation system designs. Members of the Speedster7t family support as many as eight independent GDDR6 memory ports.

Massive On-Chip Data Movement

With multiple high-speed PCIe Gen5 and 400 Gbps Ethernet ports combined with GDDR6 SDRAM interfaces, the Speedster7t FPGA family can move a tremendous amount of data directly between these various I/O ports and to the FPGAs' on-chip memory and computational resources. Speedster7t FPGAs employ both the familiar parallel interconnections of earlier FPGA generations and a 2D network on chip (NoC) to facilitate the significantly faster data-transfer rates required by future data centers.

Consider 400 Gbps Ethernet ports, which will become increasingly common in future data centers. An FPGA requires a 724 MHz, 1024-bit internal bus to handle a single, bidirectional 400 Gbps data stream. This wide bus is extremely difficult to route in a conventional FPGA switching fabric based on internal, parallel connections. Now, consider the need to handle multiple 400 Gbps Ethernet ports within a single FPGA — the requirements become even tougher. These are the sorts of data rates that the Speedster7t FPGA's on-chip NoC is designed to handle with ease.

High-Speed, On-Chip Processing Resources

FPGAs excel at processing data at high speeds due to their configurable logic and co-located SRAM resources. The Speedster7t family includes the same processing resources and memories found in previous-generation FPGAs, but adds optimizations and new processing elements to further enhance performance for many applications, including AI/ML applications.

For example, the Speedster7t FPGA incorporates new resources called machine-learning processor (MLP) blocks, which are large-scale matrix-vector and matrix-matrix multiplication engines specifically designed to accelerate AI/ML applications. MLP blocks support fixed and floating-point computations, and their resources are fracturable to support the wide range of numerical precision employed by AI/ML applications.

The MLP block architecture has been designed to exploit data-reuse opportunities that are inherent to matrix-vector and matrix-matrix multiplication. This data reuse significantly reduces the amount of data movement among memories, which increases AI/ML algorithm performance while cutting power consumption. In addition, multipliers implemented with the Speedster7t FPGA's lookup tables (LUTs) have been reformulated with the industry's most efficient modified Booth's algorithm, which doubles LUT-based multiplier performance for AI/ML algorithms.

Feature Summary

- MLP blocks with arrays of multipliers, adder trees, accumulators, and support for both fixed and floating point operations
- High-speed SerDes transceivers, supporting 112-Gbps PAM4 and 56 Gbps PAM4/NRZ modulation, as well as lower data rates
- Hard Ethernet MACs that support up to 400G
- Multiple PCIe Gen5 ports
- Network on chip (NoC) enabling high-bandwidth data flow throughout and between the FPGA fabric and hard I/O and memory controllers and interfaces
- GDDR6 and DDR5 SDRAM controllers and interfaces (AC7t1500 supports DDR4 rather than DDR5)
- New logic architecture with 6-input LUTs (6LUT), 8-bit ALUs, flip-flops, and a reformulated multiplier LUT (MLUT) mode based on a modified Booth's algorithm, which doubles the performance of LUT-based multiplication
- Fabric routing enhanced with dedicated bus routing and active bus muxing
- 72 kb BRAM and 2 kb LRAM Memory blocks

- GPIO supporting multiple I/O standards
- PLLs and DLLs to support multiple, on-chip clock trees
- Support for multiple types of programming interfaces
- Partial reconfiguration of the FPGA fabric
- Remote update of the FPGA fabric
- Security features for encrypting and authenticating bitstreams
- Debug support through Achronix's Snapshot

Family Features

Table 1: ***Speedster7t Family Overview***

Features	AC7t750	AC7t1500	AC7t3000	AC7t6000
6-input LUTs	363K	692K	1.3M	2.6M
Embedded memory	100 Mb	190 Mb	192 Mb	385 Mb
MLP blocks	336	2,560	880	1,760
SerDes 112Gbps (LR + XSR)	24 + 16	32 + 0	40 + 32	72 + 0
General-purpose I/O (GPIO)	32	64	50	100
Special-purpose I/O (SPIO)(1)	150	157	300	600
DDR5 channels	1	1(2)	2	4
GDDR6	8 channels	16 channels(3)	16 channels	16 channels
PCIe Gen5	One ×16	One ×16 and one ×8	One ×16 and one ×8	Two ×16
Ethernet	8 lanes, 2×400G or 8×100G	16 lanes, 4×400G or 16×100G	16 lanes, 4×400G or 16×100G	32 lanes, 8×400G or 32×100G

Note

1. When the DDR4 PHY is in bypass mode.
2. AC7t1500 supports DDR4.
3. This option varies by package size, see the table **Speedster7t Package and I/O Combinations** for more details.

Table 2: ***Speedster7t Package and I/O Combinations***

Package Dimensions (mm)	AC7t750	AC7t1500	AC7t3000	AC7t6000
	GDDR6, SerDes, GPIO	**GDDR6, SerDes, GPIO**	**HBM2, SerDes, GPIO**	**HBM2, SerDes, GPIO**
45×45	8 channels, 32, 32	8 channels, 32, 64		
52.5×52.5		16 channels, 32, 64	16 channels, 72, 50	16 channels, 72, 100

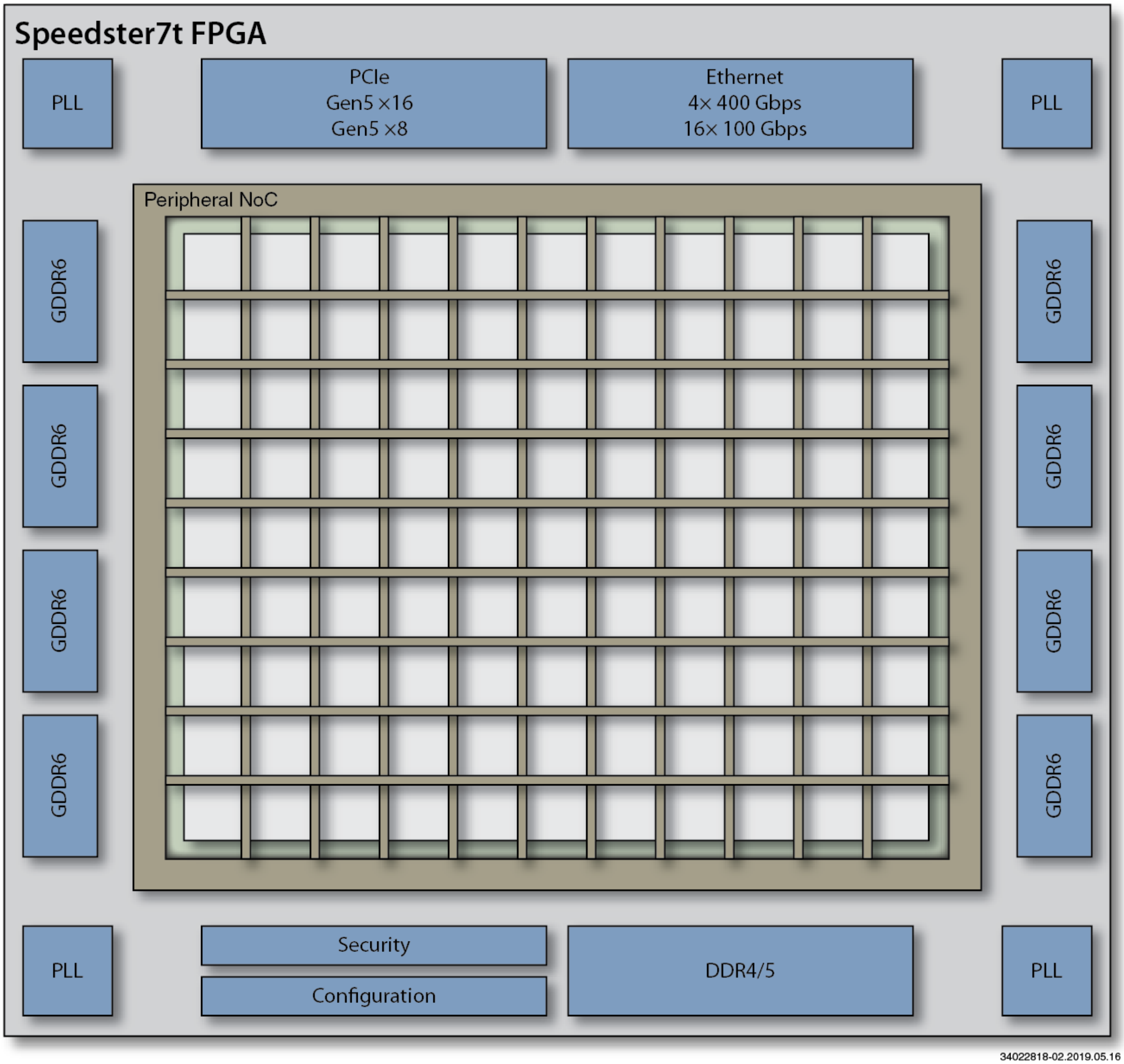


Figure 1: ***Speedster7t1500 Top-Level Block Diagram***

Chapter - 2: Speedster7t Fabric Architecture

The Speedster7t FPGA fabric is optimized for artificial intelligence and machine learning applications as well as hardware acceleration. The fabric is comprised of two main tile types: reconfigurable logic blocks (RLBs) that contain look-up tables, flip-flops, and ALUs, and machine learning processing (MLP) blocks that contain multipliers, adders, accumulators, and tightly coupled memory. The tiles are distributed as columns in the Speedster7t FPGA, and each tile consists of a routing switch box plus a logic block.

Fabric Clock Network

Speedster7t FPGAs have two types of clock networks targeted to provide both a low-skew and balanced architecture, as well as addressing the source-synchronous nature of data transfers with external interfaces.

The global clock network is the hierarchical network that feeds resources in the FPGA fabric. The global clock trunk runs vertically up and down the center of the core, sourced by global clock muxes at the top and bottom of the global trunk. The global clock network uses low-latency and low-skew distribution techniques to reach all possible endpoints in the FPGA fabric.

The second clock network, available at the periphery of the fabric, is the interface clock network. As the name implies, the intent of these clocks is to facilitate the construction of interface logic within the FPGA fabric operating on the same clock domain as external logic. Specifically, interface clocks drive the logic that communicates with the hard IP interfaces on a Speedster7t device. Interface clocks are optimized for low latency and drive logic within a specific area in the FPGA fabric.

Achronix provides dedicated clock dividers, glitch-less clock switches, and clock gates for ease of use in a customer's design. Additionally, ACE automatically provides support for inserting programmable delays at various points on a clock path to increase performance and easily facilitate timing closure.

Fabric Routing

Global Interconnect

All the tiles in the fabric are connected through the global interconnect, allowing for routing between elements, for example RLBs, MLPs, BRAMs, etc. Switchboxes in each tile act as the connection points between vertical and horizontal routing tracks. In addition to the traditional per-signal routing, the Speedster7t FPGA family introduces bus routing for high-performance data paths.

Bus Routing

The Speedster7t FPGA includes both traditional per-bit routing, as well as dedicated bus routing. The Speedster7t FPGA architecture includes separate dedicated bus-based routing for high-performance datapaths. These buses are placed into groups of up to 8 bits wide and are routed independently from standard routing in order to significantly reduce congestion.

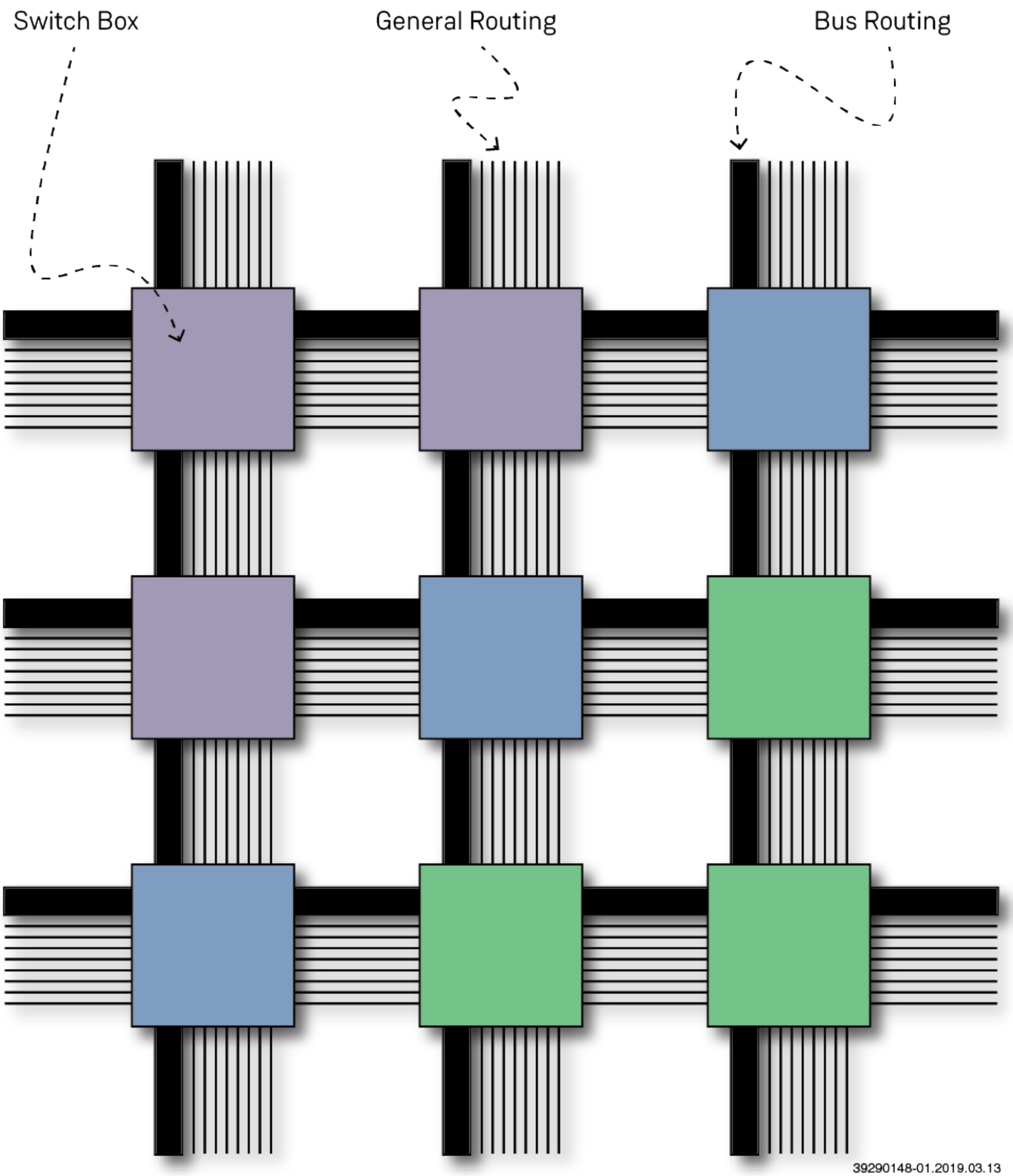


Figure 2: ***Speedster7t Bus Routing***

Additionally, the Speedster7t FPGA architecture introduces a programmable switch network for bus routing. Four 8-bit buses, one from each direction, enter each Speedster7t switchbox. Additionally, there is a 4 × 1 bus MUX for each of the 8-bit buses inside the switchbox. These bus MUXes are cascadable for wider muxing requirements. This added muxing reduces overall logic and routing resources for a design, leading to improved performance and smaller area.

Reconfigurable Logic Block (RLB)

An RLB contains 6-input look-up-tables (LUT6), a number of registers, and 8-bit fast arithmetic logic units (ALU8). The table below provides information on the resource counts inside an RLB in the Speedster7t FPGA.

Table 3: *RLB Resource Counts*

Resource	Count
LUT6	12
Registers	24
8-bit ALU	3

The following features are available using the resources in the RLB:

- 8-bit ALU for adders, counters, and comparators
- MAX function that efficiently compares two 8-bit numbers and chooses the maximum or minimum result
- 8-to-1 MUX with single-level delay
- Support for LUT chaining within the same RLB and between RLBs
- Dedicated connections for high-efficiency shift registers
- Multiplier LUT (MLUT) mode for efficient multipliers
- Ability to fan-out a clock enable or reset signal to multiple tiles without using general routing resources
- 6-input LUT configurable to function as two 5-input LUTs using shared inputs and two outputs
- Support for combining two 6-input LUTs with a dynamic select to provide 7-input LUT functionality

MLUT Mode

The RLB includes an MLUT mode for an efficient LUT-based multiplication. MLUT mode results in 2 × 2 multiplier building blocks that can be stacked horizontally and vertically to generate any size signed multiplier. For example, a 2 × 4 multiplier building block can be generated with two LUT6s, and one RLB can perform a 6 × 8 multiply.

Note

MLUT mode is supported by the MLUT generator within ACE to help customers build the multiplier desired.

Machine Learning Processor (MLP) Block

The machine learning processor block (MLP) is an array of up to 32 multipliers, followed by an adder tree, and an accumulator. The MLP can be tightly coupled with two memory blocks, a BRAM72k and LRAM2k, that can be used individually or in conjunction with the array of multipliers. The number of multipliers available varies with the bit width of each operand and the total width of input data. When the MLP is used in conjunction with a BRAM72k, the amount of data inputs to the MLP block increases along with the number of multipliers available.

The MLP offers a range of features listed below:

- Configurable multiply precision and multiplier count (any of the following modes are available)
  - Up to 32 multiplies for 4-bit integers or 4-bit block floating-point values in a single MLP
  - Up to 16 multiplies for 8-bit integers or 8-bit block floating-point values in a single MLP
  - Up to 4 multiplies for 16-bit integers in a single MLP
  - Up to 2 multiplies for 16-bit floating point with both 5-bit and 8-bit exponents in a single MLP
  - Up to 2 multiplies for 24-bit floating point in a single MLP
- Multiple number formats
  - Integer
  - Floating point 16 (including B float 16)
  - Floating point 24
  - Block floating point, a method that combines the efficiency of the integer multiplier-adder tree with the range of the floating point accumulators
- Adder tree and accumulator block
- Tightly coupled register file (LRAM) with an optional sequence controller for easily caching and feeding back results
- Tightly coupled BRAM for reusable input data such as kernels or weights
- Cascade paths up a column of MLPs
  - Allows for broadcast of operands up a column of MLPs without using up critical routing resources
  - Allows for adder trees to extend across multiple MLPs
  - Broadcast read/write to tightly coupled BRAMs up a column of MLPs to efficiently create large memories

Along with the numerous multiply configurations, the MLP block includes optional input and pipelining registers at various locations to support high-frequency designs. There is a deep adder tree after the multipliers, with the option to bypass the adders and output the multiplier products directly. In addition, a feedback path allows for accumulation within the MLP block.

Below are block diagrams showing the MLP using the fixed or floating-point formats.

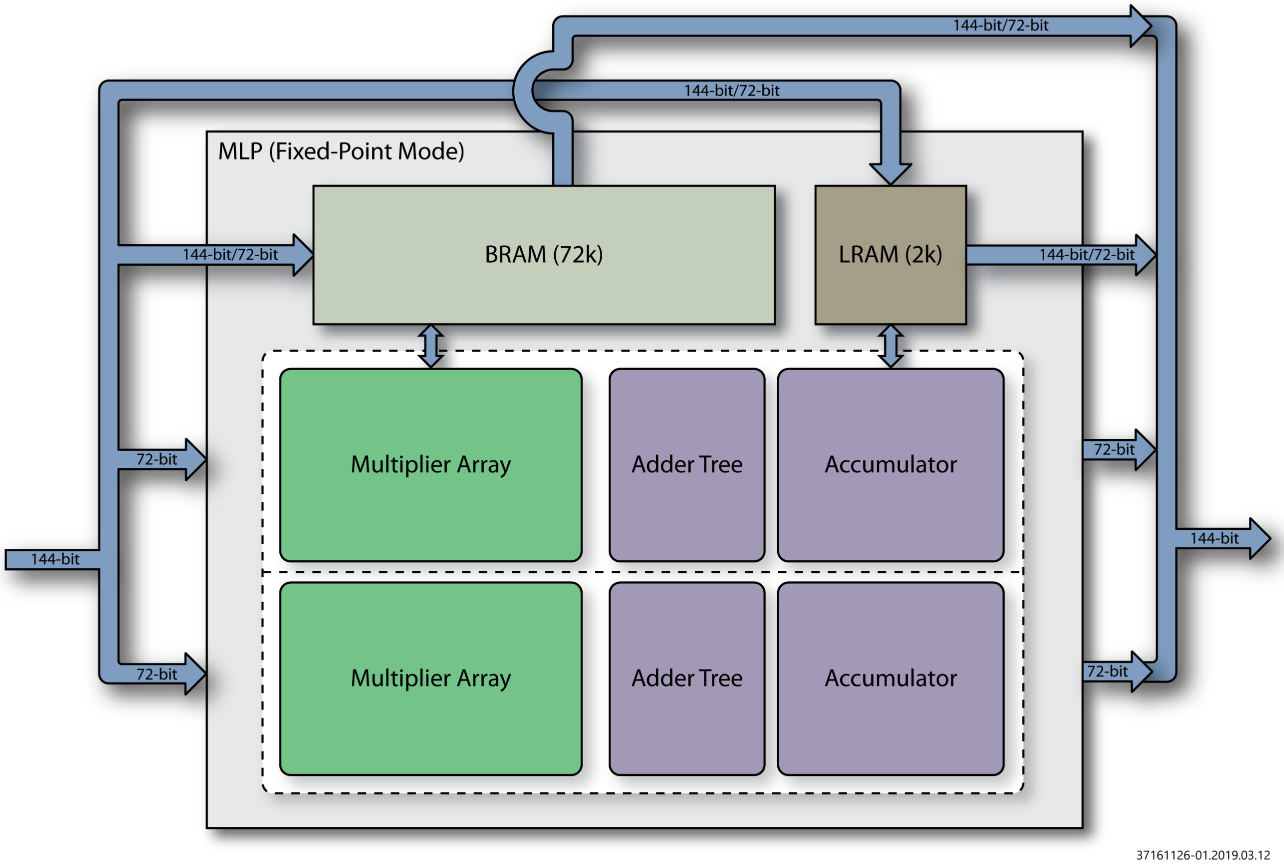


Figure 3: ***MLP Using Fixed-Point Mode***

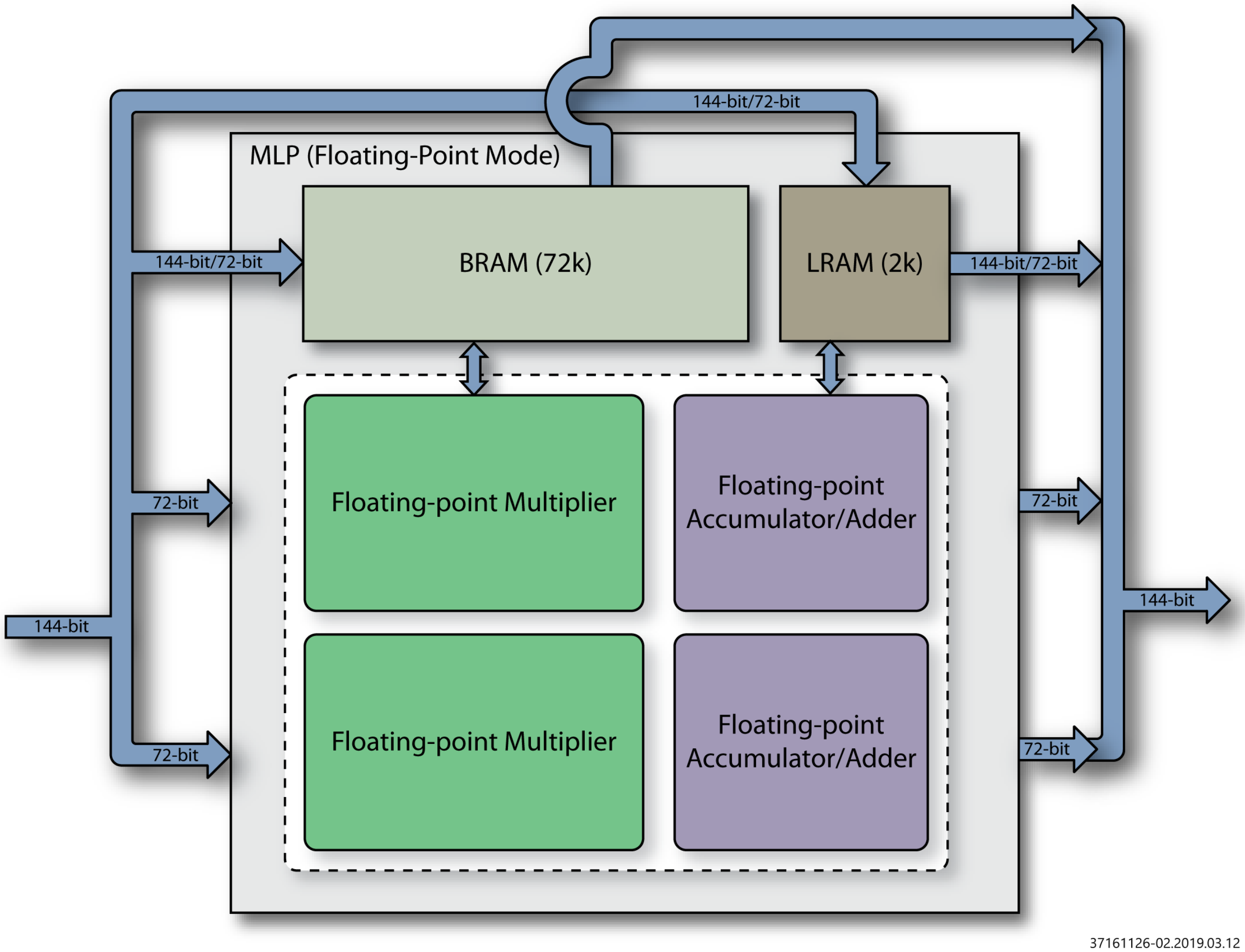


Figure 4: ***MLP Using Floating-Point Mode***

A powerful feature available in Achronix's MLP is the ability to connect several MLPs with dedicated high-speed cascade paths. The cascade paths allow for the adder tree to extend across multiple MLP blocks in a column without using extra fabric routing resources, and a data cascade/broadcast path is available to send operands across multiple MLP blocks. Cascading input or result data to multiple MLPs in parallel allows for complex, multi-element operations to be performed efficiently without the need for extra routing. Below is a diagram showing the cascade paths across MLPs.

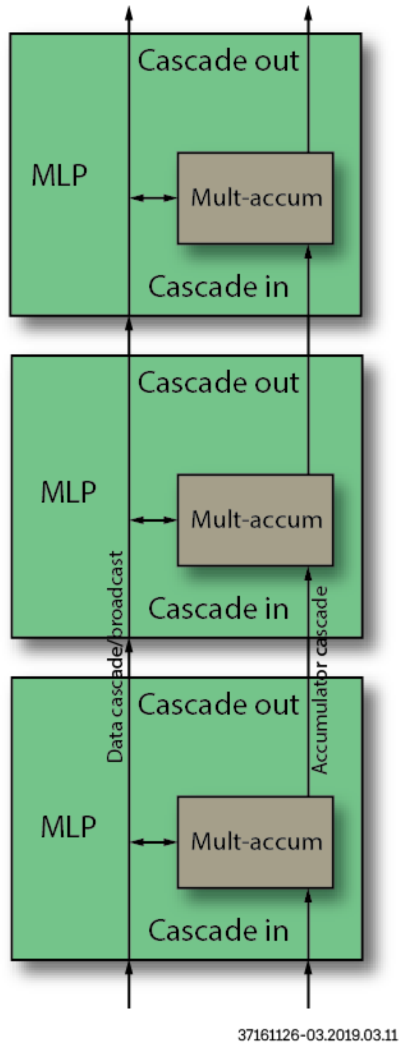


Figure 5: ***MLP Cascade Path***

Block RAM 72k (BRAM72k)

The BRAM72K primitive implements a 72-kb simple-dual-port (SDP) memory block with one write port and one read port. Each port can be independently configured with respect to size and function, and can use independent read and write clocks. The BRAM72K can be configured as a simple dual port or ROM memory. The key features (per block RAM) are summarized in the table below.

Table 4: ***BRAM72K Key Features***

Feature	Value
Block RAM size	72 kb
Organization	512 × 144, 128 × 512, 1024 × 72, 1024 × 64, 2048 × 36, 2048 × 32, 4096 × 18, 4096 × 16, 8192 × 9, 8192 × 8, or 16384 × 4

Feature	Value
Physical Implementation	Columns throughout device
Number of Ports	Simple Dual Port (independent read and write)
Port Access	Synchronous writes, synchronous reads, write and read clock can be asynchronous to each other
FIFO	Built-in FIFO controller with dedicated pointer and flag circuitry

The BRAM72K ports are Illustrated in the following figure:

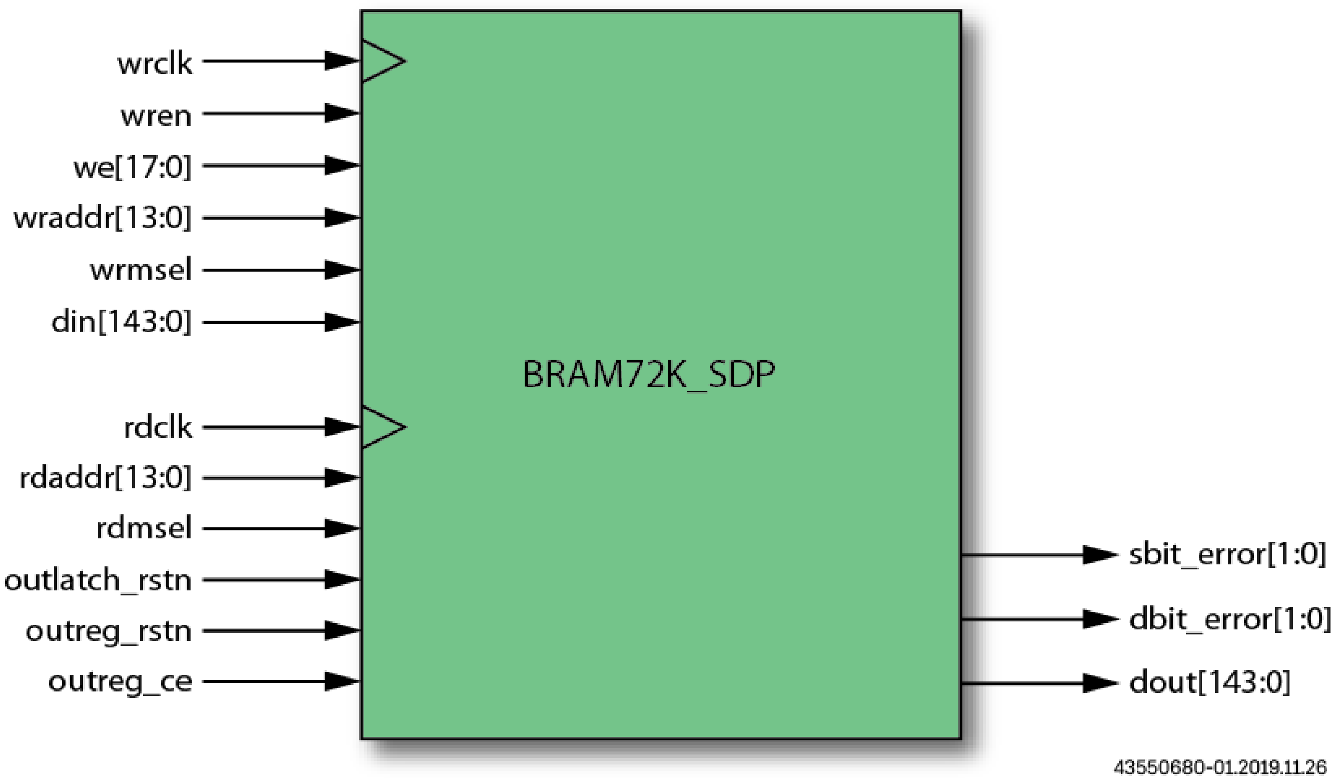


Figure 6: ***BRAM72K Block Diagram***

Logic RAM 2k (LRAM2k)

The LRAM2K implements a 2,304-bit memory block configured as a 32 × 72 simple dual-port (one write port, one read port) RAM. The LRAM2K has a synchronous write port. The read port is configured for asynchronous read operations with an optional output register. A summary of LRAM2K features is shown in the table below.

Table 5: *LRAM2K Key Features*

Feature	Value
Logic RAM size	2,304 bits
Organization	16 × 144, 32 × 72 or 64 × 36 (depth × width)
Physical Implementation	Columns throughout device
Number of Ports	Simple dual port (one read, one write)
Port access	Synchronous writes, combinatorial reads
FIFO	Built-in FIFO controller with dedicated pointer and flag circuitry

The LRAM2K ports are shown in the following figure:

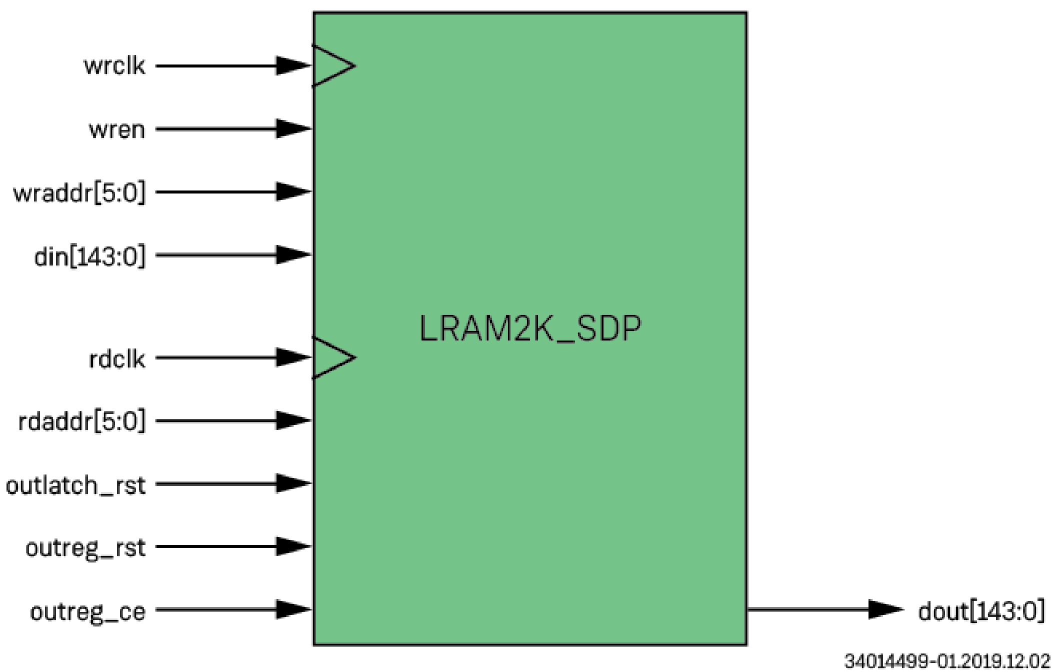


Figure 7: *LRAM2K Block Diagram*

Chapter - 3: Speedster7t FPGA I/O and PHY

Speedster7t FPGAs have a variety of I/O and PHY to communicate with external components.

112 Gbps SerDes

Speedster7t FPGAs provide high-speed serial transceivers which can be used for interface protocols running from 1 Gbps up to 112 Gbps. They are designed to support NRZ and PAM4 data-center standards. The Speedster7t FPGA provides a PCS and PMA to support the needs of many common high-speed serial protocols.

PMA Features

- Data rates from 1 Gbps to 112 Gbps
- DC coupling or external AC coupling
- Lock to reference clock or data
- Support for oversampling
- BIST with near/far-end loopback and PRBS 7, 13, 15, 23, 31 generator/checker
- Eye monitor

PCS Features

- Data rates from 1 Gbps to 112 Gbps using Ethernet subsystem, 1 Gbps to 56 Gbps raw SerDes
- Supports data path widths of 16, 20, 32, 40, 64, and 128 bits
- 8b/10b encoding/decoding support for PCIe 16, 20, and 32-bit internal data paths
- Comma detection and byte/word alignment for PCIe 8b/10b
- 128b/130b encoding/decoding support for PCIe Gen3/Gen4/Gen5 32 and 64-bit internal data path
- Elastic receive buffer for clock compensation and channel bonding
- Support for 66b/64b CAUI gearbox in both synchronous and asynchronous mode
- Support for 67b/64b gearbox in synchronous mode
- Native support for Ethernet 1G/10G/25G/50G/100G, XAUI, CPRI, Jesd4C, SyncE, and Interlaken
- Bypass mode for PCS (bypasses the PCS)

GPIO

Speedster7t FPGAs provide general-purpose I/O (GPIO) pins to enable communication with external components. These GPIO support multiple I/O standards at multiple voltages.

The table below lists the supported I/O standards. There are separate clock I/O banks, which are described in the next section.

Table 6: ***Supported General-purpose I/O Standards***

I/O Standard Supported	Supported Voltage (V)	Single-Ended/Differential
HSTL Class I	1.5	single-ended, differential
	1.8	
HSTL Class II	1.5	
HSUL	1.2	
LVCMOS	1.1	
	1.2	
	1.5	
	1.8	
SSTL Class I	1.2	
	1.35	
	1.5	
	1.8	
SSTL Class II	1.8	

Special-Purpose I/O (SPIO)

The DDR4 subsystem in the Speedster7t1500 FPGA can be utilized in two modes: PHY bypass or regular. In the PHY bypass mode where the DDR4 interface is not being used, the user can access all DDR4 I/O as special-purpose I/O. The DDR4 I/O can be utilized either in regular PHY mode for DDR4 memory interfacing or in PHY bypass mode, but a combination of the two is not allowed. The SPIO:

- Can drive low-frequency interfaces running at a maximum of 100 Mhz.
- Are not compliant with a specific industry I/O standards. These I/O operate at 1.2V (±5%).
- Maintain the signal direction of the DDR4 interface.
- Can supply up to 157 additional I/O.

Clock I/O

Speedster7t FPGAs provide two types of clock I/O pins to enable communication with external components:

- MSIO – Clock I/O that support multiple I/O standards at multiple voltages.

- REFIO – Clock I/O that support LVCMOS, LVDS, and LVPECL.

The table below lists the supported I/O standards for each clock I/O type.

Table 7: ***Supported Clock I/O Standards***

I/O Standard Supported	Supported Voltage (V)	Single-Ended/Differential
MSIO		
HSTL Class I	1.5	single-ended, differential
	1.8	
HSTL Class II	1.5	
LVCMOS	1.5	
	1.8	
SSTL Class I	1.5	
	1.8	
SSTL Class II	1.8	
REFIO		
LVCMOS	1.5	single-ended, differential
	1.8	
LVDS	1.5	differential
	1.8	
LVPECL	1.5	
	1.8	

PLLs

There are sixteen general purpose PLLs, four in each corner of the Speedster7t FPGA. They are fractional-N divide and spread-spectrum PLLs, supporting a wide range of frequencies with excellent jitter performance. The general-purpose PLLs can be used to drive low-skew, high-speed clocks to nearby I/O, the global clock network, and interface clocks in the FPGA fabric.

Below is a list of features available in the PLLs:

- Programmable PLL with fractional-N divide and spread-spectrum clock generation
- Wide range of output frequencies supported: 7.5 MHz to 2 GHz

- Reference clock from dedicated clock I/O, adjacent PLLs (for cascading PLLs), as well as clock pins and PLLs from other device corners
- Up to four output clocks
- Reference clock and output clock dividers
- Output duty cycle 50%
- Low jitter
- Low power

Note

ACE currently supports the programmable fractional-N divide. Spread-spectrum is not configurable at this time.

Table 8: ***Details of PLL***

Parameter	Min	Max	Units
Reference frequency	10	600	MHz
Output frequency	7.5†	2000	MHz
Maximum long-term jitter	±2% divided reference clock		

† 0.93MHz minimum frequency after divider

DLLs

In each corner of a Speedster7t FPGA there is one master DLL with eight slaves available for the phase shifting of clocks. This arrangement allows for one master clock and up to eight slave clocks that can be phase shifted based on the master clock's frequency.

The programmable DLLs provide precise phase alignment between output clocks, deskew signals relative to a clock, and includes features such as spread-spectrum support. The DLLs are configured along with the PLLs located in the same corner of the device. Below is a list of features supported in the programmable DLLs:

- Supports 300-1333 MHz
- 256 taps
- Lock detection
- Power-down mode when not used in the design
- Supports holding DLL in reset
- Available output test clock
- Control and status register read back

Chapter - 4: Speedster7t FPGA Network On Chip

The Speedster7t FPGA family of devices has a network hierarchy that enables extremely high-speed dataflow between the FPGA core and the interfaces around the periphery, as well as between logic within the FPGA itself. This on-chip network hierarchy supports a cross-sectional bidirectional bandwidth of 20 Tbps. It supports a multitude of interface protocols including GDDR6, DDR4/5, 400G Ethernet, and PCI Express Gen5 data streams, while greatly simplifying access to memory and high-speed protocols. Achronix's network on chip (NoC) provides for read/write transactions throughout the device, as well as specialized support for 400G Ethernet streams in selected columns.

Master Endpoints

- 80 NoC access point (NAP) masters distributed throughout the FPGA core for user-implemented masters
- Two PCI Express Interfaces
- FPGA configuration unit (FCU)

Slave Endpoints

- 80 NAP slaves distributed throughout the FPGA core for user-implemented slaves
- 16x GDDR6 slave interfaces
- DDR4/5 controller
- Two PCI Express Interfaces
- All control and status register (CSR) interfaces of all subsystem cores
- FCU (to enable configuring of FPGA and interface subsystems)

Packet Endpoints

- 80 vertical and 80 horizontal NAP packet interfaces distributed throughout the FPGA core for fabric-to-fabric transactions
- 32 of the 80 vertical NAPs can send and receive data to/from the Ethernet subsystems, each Ethernet controller connects to two dedicated NoC columns
- Two Ethernet subsystems, supporting a mix of up to 4× 400 Gbps Ethernet or 16× 100 Gbps Ethernet

NoC Features

The NoC provides a method to easily connect high-bandwidth interfaces to the FPGA fabric, as well as enabling communication between memory and high-speed protocols. To make these high-bandwidth connections both flexible and easy to use, the NoC provides the following features.

Table 9: ***NoC Features***

Feature Summary	Feature Description
NoC-FPGA Interface Modes	The NoC-to-FPGA access point (NAP) supports the following modes: • AXI 256b slave mode • AXI 256b master mode • Ethernet and NAP-to-NAP data streaming mode
NoC Address Decoding	The NoC has a global address map and handles all address decoding on transactions, making it easy for the user to send transactions from one endpoint to another.
NoC Memory Address translation and Firewall	The NoC implements an address translation table for each NAP. This allows the FPGA design to control how the global memory space is arranged for each NAP, and allows access to specific memory regions to be blocked for security, also on a per-NAP basis.
NoC Forwarding Latency	1 to 2 ns of latency from one NAP to the next on the same row or column respectively.
NoC Flow Control	The NoC manages flow control internally, such that data is never dropped. Users have the option to configure their own priority weights per NAP to control the round-robin flow control which affects congestion and latency.
NoC Security	The NoC implements address translation tables to support security.

The NoC extends both vertically and horizontally until reaching the edge of the device. The diagram below shows the connections between the peripheral portion of the NoC, the high-bandwidth interfaces, and the columns and rows of the NoC. As shown, the Ethernet has dedicated connections of up to 400G to specific columns of the NoC. The PCIe ×16 and ×8 connect to the periphery of the NoC at 512 Gbps and 256 Gbps respectively. For GDDR6, the NoC can achieve bandwidth of up to 2 Tbps over the full group of GDDR6 interfaces on each side of the device. The columns and rows of the NoC can move traffic to/from the user logic in the fabric at up to 512 Gbps in each direction.

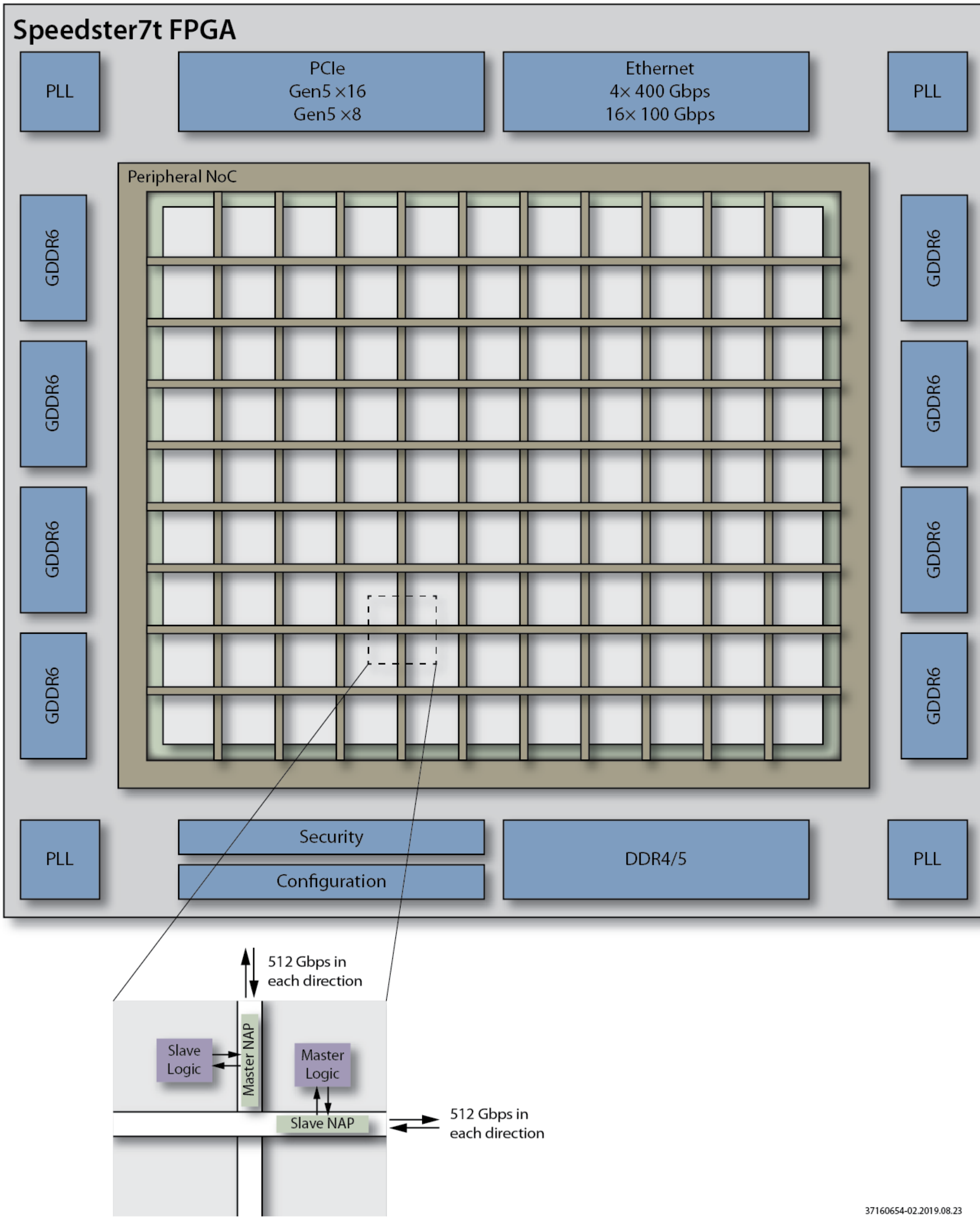


Figure 8: ***Speedcore7t NoC Showing Master and Slave Endpoints***

Columns and Rows of the NoC

The NoC is composed of regularly spaced node elements at the center of each cluster throughout the core fabric of the FPGA. The NoC nodes provide connectivity to adjacent nodes in both the horizontal and vertical directions. Each horizontal and vertical link within the NoC supports 512 Gbps throughput in both directions.

The NoC transaction mapping logic is optimized for AXI read and write transactions. User master logic implemented in the FPGA core can issue AXI read or write transactions to the NAP's AXI slave, and the NoC row carries the transaction to the east or west boundary of the FPGA core to be issued to the deep DDR4/5 memory interface or one of the high-speed GDDR6 memory interfaces. PCIe transactions arriving from the north side of the device are issued to the NoC columns, which transport the transaction requests down the columns to user slave logic in the FPGA.

Each row and column is able to support a full 512 Gbps of traffic.

The rows and columns of the NoC support both transactional and non-transactional data transfers such as streams of data.

- **Transactional data transfer** – This type of transfer includes AXI read and write commands, data, and responses. The command transfers are typically a single cycle, and data transfers are typically short taking only a few cycles.
- **Non-transactional data transfer** – This type of transfer pushes data streams through the NoC like a FIFO. It is a point-to-point data transfer and is used in two types of transfers:
  - Ethernet – This transfer allows data to be bundled as longer streams of data. Data is sent down selected columns from Ethernet to a specific NAP on the column.
  - NAP-to-NAP – The NoC allows the user to send data between NAPs within the same column or the same row. In this mode, streams of data are transferred from endpoint to endpoint without further processing.

Peripheral NoC

The peripheral portion of the NoC carries transactions between the FPGA core and the peripheral IP blocks. The NoC can also carry transactions directly between the different peripheral IP blocks. The NoC provides the following services:

- Address decoding
- Transaction command and response routing
- Width adaptation
- Frequency adaptation (clock domain crossing)
- Burst adaptation
- Protocol conversion (e.g., AXI to/from APB)

The peripheral portion of the NoC only carries read and write transactions. It does not carry Ethernet packets or data from SerDes.

Each row of the NoC presents an AXI master to the periphery of the NoC on both the west and east side of the FPGA core. Similarly, each column of the NoC presents an AXI slave to the periphery of the NoC on both the north and south side of the device. This structure allows user logic to read or write any external IP or control and status register (CSR) interface and allows any external IP with a master interface to access any slave endpoints with attached user logic.

The NoC on a Speedster7t FPGA has two important features:

- The NoC is usable immediately when reset is released, without configuration of any control and status registers, the FPGA fabric, or the IP interfaces.
- After configuration of IP interfaces and/or control and status registers, the NoC supports transfers between IP cores (such as PCIe and GDDR6) without requiring the FPGA fabric to be configured.

Connectivity Between NoC and Endpoints on FPGA

The connectivity between the NoC and the different endpoints on the FPGA device can be categorized into three scenarios: NoC-to-user logic connectivity, NoC-to-interface IP connectivity, and NoC-to-FCU connectivity.

NoC-to-User Logic Connectivity

A NoC access point (NAP) needs to be instantiated in the user design in order to gain access to the rows and columns of the NoC. There is a NoC column with a master NAP and a slave NAP in each cluster. To the FPGA core, these access points look like any other logic columns in the FPGA fabric. The FPGA core provides a clock to the NAP as it does for any other column type. Internally, the NAP has an asynchronous FIFO used to adapt the data rates to what the FPGA can achieve.

NoC-to-Interface IP Connectivity

The NoC enables any NoC access point (NAP) in the FPGA to access any Interface IP slave, including any of the GDDR6 AXI interfaces and any of the DDR4/5 or PCIe controllers. It is also feasible to access the control and status interfaces of every IP core, DLL/PLL, and the FCU, through the NoC.

DDR4/5 and GDDR6 Connectivity

Each memory interface presents a 256-bit slave interface to the NoC and accepts read or write transactions. Multiple NoC access points can issue transactions to a single memory interface to utilize the full bandwidth provided by the high-speed memory interfaces.

PCI Express Connectivity

PCIe masters and slaves are connected directly to the NoC.

PCIe includes a second interface that does not connect to the NoC, but instead is a direct connection to the FPGA fabric. This interface supports up to Gen4 PCIe.

NoC-to-FCU Connectivity

The fabric configuration unit (FCU) can issue transactions to the NoC, allowing the configuration logic to set any CSR interface on the device. Agents on the NoC, such as FPGA logic and the PCIe master can issue commands to the FCU, allowing for configuration over PCIe and other useful features.

Chapter - 5: Speedster7t FPGA Interface Subsystems

The Speedster7t FPGAs have dedicated, hard interfaces to support the latest and most advanced versions of serial and memory interfaces used in high-performance networking and compute offload applications including 400G Ethernet, PCI Express Gen5, GDDR6, and DDR4 or DDR5. The combined interfaces exceed 10 terabits per second of total device bandwidth.

Ethernet

Speedster7t FPGAs include an Ethernet subsystem consisting of 8 SerDes lanes and Ethernet MACs to support a combination of applications. The Ethernet MAC is very flexible and can support multiple ports up to 400G, with each SerDes lane able to achieve a line rate between 10G and 100G. The Ethernet subsystem connects to the FPGA fabric through the network on chip (NoC). The table below lists the supported applications.

Table 10: ***Multi-rate Ethernet Modes Supported per Subsystem***

Mode	Number of Channels	SerDes Rate (Per Lane)	SerDes Lanes
400G	Up to 2	100G	4 lanes each channel
	1	50G	8 lanes
200G	Up to 2	50G	4 lanes each channel
	Up to 4	100G	2 lanes each channel
100G	Up to 2	25G or 26.5G	4 lanes each channel (KR4 or KP4)
	Up to 4	50G	2 lanes each channel
50G	Up to 4	25G	2 lanes each channel
40G	Up to 2	10G	4 lanes each channel
	Up to 4	20G	2 lanes each channel
10G/25G/50G/100G	Up to 8	10G, 25G, 50G, 100G	Independent single-lane applications

For information on the number of Ethernet subsystems available in a device, see the Speedster7t Family Overview (see page 9) table.

Additional Features

- Support for Reed-Solomon FEC (RS-FEC) implementing RS(528, 514) and RS(544, 514) for 100G-KR and 100G-KP applications respectively, as well as 25G and 50G applications
- Support for RS(272, 258) low-latency variant for up to 100G

- Support for 15G (Clause 108) and 50G (Clause 134) and 25/50G Ethernet Consortium specifications
- Configurable Base-R PCS compliant with IEEE 802.3 Clauses 49, 82, 107, 133 for 10G, 25G, 50G operation respectively
- Independent 64bit XLGMII MAC interfaces per channel
- Support for error indication to PCS when uncorrectable errors are detected
- 1588 I-step for 10G up to 100G, 200G, and 400G
- The IEEE 802.3br supported, providing two transmit and receive interfaces for 10G up to 100G
- Optional support for energy efficient Ethernet (EEE) fast-wake (i.e. transfer of LPI sequences, no deep-sleep)
- Optional Base-R (Firecode) FEC according to Clause 74 of IEEE 802.3
- TSN support for 100G and below (IEEE 802.1 Time Sensitive Networking, and IEEE 802.3br Interspersing Express Traffic)
- Interface for register configuration

PCI Express

Speedster 7t FPGAs have two PCIe interfaces. The first interface supports up to 16 lanes (×16). The second PCIe interface supports up to 8 lanes (×8). Both PCIe controller interfaces support dual-operation, as either an endpoint or as a root complex.

Table 11: *Speedster7t PCIe Interface Specifications*

Feature	PCIe Port 1	PCIe Port 2
PCI Express Specification	Revision 5.0, Version 0.9	Revision 5.0, Version 0.9
PIPE	Version 5.1.1	Version 5.1.1
Maximum width	×16	×8
Maximum throughput	512 GTs (Gen 5)	256 GTs (Gen 5)
Supported functionality	Root-Port + End-Point	Root-Port + End-Point
DMA support	Yes	Yes
DMA read channels	4	2
DMA write channels	4	2
BAR	4	4
Virtual channels	1	1
Physical functions	4	2
Virtual functions	252	0

Feature	PCIe Port 1	PCIe Port 2
Advanced error reporting (AER) support	Yes	Yes
IOV	256	None

GDDR6

Speedster7t devices contain GDDR6 subsystems on the west and east sides of the device to provide external high-bandwidth memory interface support. The controller and PHY implementation are compliant with the JEDEC GDDR6 SGRAM Standard JESD250. See the table below for a summary of the key specs and features.

Each GDDR6 interface operates on two channels, each of which can be disabled independently. The controller supports a wide range of features, including bus utilization optimization, page-hit mitigation, multiport front end (MPFE), reordering and error interrupt.

The GDDR6 subsystems can run up to a data rate of 16 Gbps with device densities from 8 Gb to 16 Gb. The implementation supports GDDR6 up to ×16 in non-clamshell modes and up to ×8 in clamshell modes.

The GDDR6 controller connects to the other interface subsystems on the Speedster7t device via the NoC. Additionally, the GDDR6 subsystems can connect directly to the FPGA fabric via an AXI interface with support for full or half-rate clocking. The FPGA fabric and other subsystems can connect to GDDR6 in the following ways:

- A 256-bit AXI interface to the network on chip (NoC), which can run up to 1 GHz, and connects to interface subsystems and FPGA fabric.
- A 512-bit AXI direct-to-fabric interface, which can run up to 500 MHz.

Users can configure the PHY ZQ calibration as Master/Slave mode across multiple PHY’s.

Furthermore, the IP comes with a memory test and analyzer core to enable standalone testing of the controller and memory during board bring up.

Table 12: ***GDDR6 Key Specs and Features on Speedster7t***

GDDR6 Feature	Support in Speedster7t Devices
Memory suppliers	Micron, Samsung, SK Hynix
Maximum number of memory chips per FPGA	8 (clamshell), 16 (non-clamshell)
Maximum total capacity	16GB (1×16 Gb chips in non-clamshell mode) 16GB (2×8 Gb chips in clamshell mode)
Number of channels per chip	2
Maximum number of channels total per FPGA	16
Width per channel (bits)	16
Maximum per-pin data rate supported by FPGA	16 Gbps
Maximum total bandwidth (No_of_channels_per_FPGA × width_per_channel × rate)	4.0 Tbps
Capacity per memory chip	8 Gb – 16 Gb
Total memory per FPGA	Up to 16GB
Memory data rates	12 Gbps, 14 Gbps, 16 Gbps

DDR4/DDR5

Speedster7t devices include DDR5 interfaces (DDR4 in the AC7t1500), ensuring that memory capacity requirements can be satisfied across a vast application space. The DDR4/5 PHY and controller in Speedster7t devices are compliant to the DDR4/5 JEDEC specification and can operate up to 3200 Mbps in ×4, ×8 and ×16 width configurations. The implementation supports component memories, UDIMM/SO-DIMM form factors as well as RDIMMs and LRDIMMs. See the table below for a summary of the key specifications and features.

Speester7t devices allow for multi-rank support in the DDR4/5 interfaces, up to 4 in standard mode, and up to 16 in 3DS mode.

The DDR4/5 PHY/controller can connect to the other interface subsystems or FPGA fabric via an AXI interface with support for full, half and quarter-rate clocking. The two connectivity options include:

- A 256-bit AXI interface to the network on chip (NoC), which can run up to 800 MHz, and connects to interface subsystems and FPGA fabric.
- A 512-bit AXI direct-to-fabric interface, which can run up to 400 MHz.

Speedster7t devices support AXI compliant low-power interfacing. The DDR4/5 PHY/controller provides three options for low-power mode:

- 256-bit AXI interface in low power
- 512-bit AXI interface in low power

- Memory controller core logic in low power

Users also have the option to bypass the entire DDR4/5 PHY and use these I/O for driving low-performance interfaces such as I^2C, or for optics control, LEDs, etc.

Table 13: *DDR4/5 Key Specifications and Features on Speedster7t Devices*

DDR4/5 Feature		Support in Speedster7t Devices
Memory types		Component, UDIMM/SO-DIMM, RDIMM, LRDIMM
Memory configurations		×4, ×8, ×16
Maximum data rate		3200 Mbps
Burst modes		BL8, burst chop
Data path widths	Non-ECC	8-bit, 16-bit, 32-bit, 64-bit
	ECC	32-bit + 7-bit ECC, 64-bit + 8-bit ECC
Multi-rank support		4 (standard), 16 (3DS)
AXI interface		AXI4 with read reorder buffer and port data widths of 256 and 512 bits
Testability and characterization		Built-in scan, loopback, delay line, PLL, auto-timing and ATE read tests.

Chapter - 6: Speedster7t FPGA Configuration

For normal operation, the Speedster7t FPGA core requires configuration by the end user. Speedster7t devices can be configured via one of four interfaces:

- Flash
- JTAG
- CPU
- PCI Express (PCIe)

A configuration bitstream is generated in ACE by selecting the appropriate configuration interface. The configuration mode of the FPGA is controlled via mode select pins on the configuration interface of the FPGA. These pins can be driven via hardware on the board or by another device such as a CPLD. The user has the option to generate an encrypted and authenticated bitstream. If this feature is used, the Speedster7t device first secures the hardware and then authenticates and decrypts the bitstream before programming the FPGA fabric.

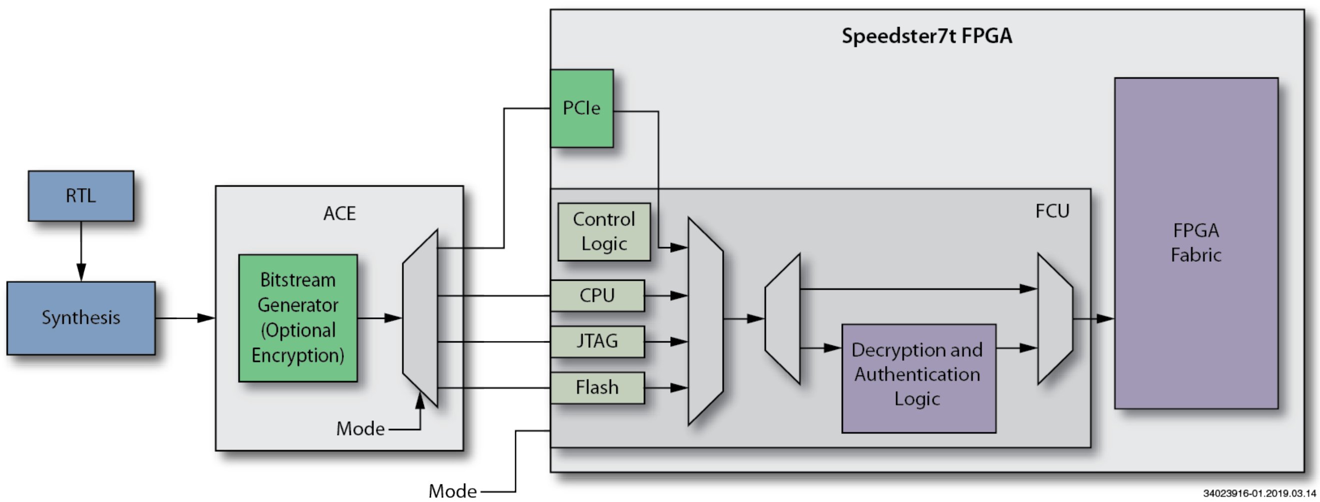


Figure 9: *Bitstream Generation and Configuration Process*

Flash Mode

The serial flash programming mode allows flash memories to be used to configure the Speedster7t FPGA. In this mode the Speedster FPGA is the master, and therefore, supplies the clock to the flash memory. Flash programming supports SPI (single-bit interface to the flash memory), dual (two-bit interface to the flash memory), quad (four-bit interface to the flash memory) and octa (eight-bit interface to the flash memory) modes. Additionally, the Speedster7t FPGA can interface to one device (1D) or four devices (4D) of flash memory modules on the board. The bitstream size is entirely dependent on the size of the fabric. It is important that the flash solution chosen is large enough to store the bitstream data.

Flash mode also supports the remote update with fallback option feature, wherein the user can simultaneously store two bitstreams in the flash device and choose to program the FPGA from either one. The update can be triggered remotely via a user application that writes to appropriate registers on the Speedster7t device. If bitstream programming fails for some reason, the fallback logic loads a known good bitstream which allows the device to resume normal operation.

JTAG Mode

The Speedster7t JTAG Tap controller is IEEE Std 1149.1 and 1149.6 (AC JTAG) compliant. The JTAG interface also provides debug capability for Achronix's on-chip logic analyzer tool, Snapshot, and other debug tools. The Speedster7t FPGA can be configured as a single JTAG device, or as part of a series of cores within a system connected on the JTAG chain.

CPU Mode

In CPU mode, an external CPU acts as the master and controls programming operations. This mode offers a high-speed method for loading configuration data. Depending on the pin settings, CPU mode is either a 1-, 8-, 16-, 32-, or 128-bit wide parallel interface. This mode provides for the widest data interface and a maximum supported clock rate of 250 MHz.

> **Note**
>
> The 128-bit mode shares pins with the DDR interface. This interface is disabled when using 128-bit mode.

PCIe Mode

PCIe mode requires two-stage programming. First, the I/O ring portion of the Speedster7t device is configured via flash, JTAG, or CPU. Once the PCIe interface is enabled, bitstream programming is performed via indirect addressing, where the AXI slave interface in the Speedster7t FPGA receives the bitstream in the form of a PCIe packet and writes that data to the programming registers.

Bitstream Security Features

Achronix recognizes the importance of protecting the sensitive IP a customer downloads onto their FPGA. To provide a high level of protection, Speedster7t FPGAs have a number of features to support bitstream encryption as well as authentication. These features ensure that no one can access the design configuration on the FPGA and also ensures that the design is the intended design. Speedster7t FPGAs provide this high level of security through the following features:

- Support for RSA authenticated and AES-GCM encrypted bitstream
- Dynamic power analysis (DPA) protection to prevent side-channel attacks
- Physically unclonable function (PUF) for tamper-proof protection
- Securely stores both public and encrypted private keys

With this security solution deployed, a customer's design is secure. Even with possession of the device, no one can extract the underlying design, the design cannot be reverse engineered, nor can the design be altered in any way.

Chapter - 7: Speedster7t FPGA Debug

JTAG Browser View

The JTAG Browser view provides the user with an interactive means of inspecting and modifying registers within the active design on an FPGA over the JTAG interface. (The acx_stapl_player and Bitporter pod or FTDI FT2232H JTAG device perform the JTAG interactions; see the *Bitstream Programming and Debug User Guide (UG004)* for more information.)

After choosing the Target Device and the IP Block within that device, the user is able to browse and edit registers on a live device. All accessible IP blocks on the FPGA are selectable from a pull down list; once selected, the attributes (base-address, end-address, word-size, etc) for the selected IP block are displayed, along with the acx_stapl_player commands which will be used to read and write to the block's registers.

Snapshot

Snapshot is the real-time design debugging tool for Achronix FPGAs and cores. The Snapshot debugger, which is embedded in the ACE software, delivers a practical platform to observe the signals of a user's design in real-time. To use the Snapshot debugger, the Snapshot macro needs to be instantiated inside the user's RTL. After instantiating the macro and programming the device, the user will be able to debug the design through the Snapshot Debugger GUI within ACE, or via the `run_snapshot` TCL command API.

The Snapshot macro can be connected to any logic signal mapped to the Achronix core, to monitor and potentially trigger on that signal. Monitored signal data is collected in real time in regular BRAMs, prior to being transferred to the ACE Snapshot GUI. The Snapshot macro has configurable monitor width and depth, as well as other configuration parameters, to allow user control over resource usage. The ACE Snapshot GUI interacts with the hardware via the JTAG interface: interactively specified trigger conditions are transferred to the design, and collected monitor data is transferred back to the GUI, which displays the data using a builtin waveform viewer.

The figure below shows the components involved in a Snapshot debug session.

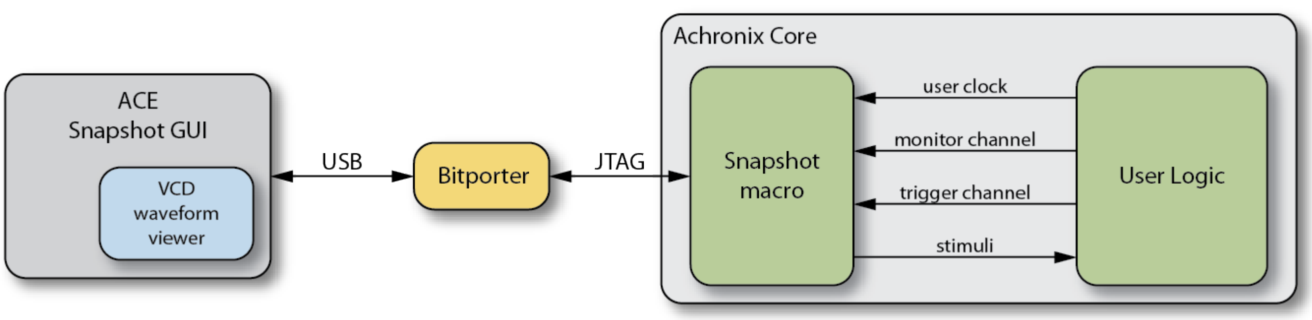


Figure 10: *Snapshot Overview*

Features

The Snapshot macro samples user signals in real time, storing the captured data in one or more BRAMs. The captured data is then communicated through the JTAG interface to the ACE Snapshot GUI.

The implementation supports the following features:

- Monitor channel capture width of 1 to 4064 bits of data.
- Monitor channel capture depth of 512 to 16384 samples of data at the user clock frequency.
- Trigger channel width of 1 to 40 bits.
- Supports up to three separate sequential trigger conditions. Each trigger condition allows for the selection of a subset of the trigger channel, with AND or OR functionality.
- Bit-wise support for edge- (rise/fall) or level-sensitive triggers.
- The ACE Snapshot GUI allows specification of trigger conditions and circuit stimuli at runtime.
- An optional initial trigger condition, specified in RTL parameters, to allow capture of data immediately after startup, before interaction with the ACE Snapshot GUI.
- A stimuli interface, 0 to 512 bits wide, that allows the user to drive values into the Achronix core logic from Snapshot. Stimuli values are specified with the ACE Snapshot GUI and made available before data capture.
- Optionally, the data capture can include values before the trigger occurred. This "pre-store" amount can be specified in increments of 25% of the depth.
- Captured data is saved in a standard VCD waveform file. The ACE Snapshot GUI includes a waveform viewer for immediate feedback.
- The VCD waveform file includes a timestamp for when the Snapshot was taken.
- ACE automatically extracts the names of the monitored signals from the netlist, for easy interpretation of the waveform.
- A repetitive trigger mode, in which repeated Snapshots are taken and collected in the same VCD file.
- The JTAG interface can be shared with the user design.
- A TCL batch/script mode interface is provided via the `run_snapshot` TCL command

Chapter - 8: Speedster7t FPGA Timing Data

Speed Grades

The core voltage for Speedster7t FPGAs vary by device speed grade (refer to the table, Speedster7t Speed Grades (see page 46)).

Speedster7t AC7t1500 (Commercial Temperature Range: 0°C to +85°C)

SerDes (Standard Mode/Ethernet Mode)

SerDes data/clock at parallel ports go to Ethernet/PCS controller directly.

Table 14: ***SerDes Maximum Clock Rates (Standard Mode/Ethernet Mode)***

Clock	Description	Speed Grade			Units
		3	2	1	
tx_block_clk	SerDes transmit clock at the parallel ports	830			MHz
rx_block_clk	SerDes receive clock at the parallel ports	830			MHz
ck_tx_quad	PCS clock for SerDes quad	830			MHz
ck_tx_block	PCS clock for SerDes block	830			MHz

Table 15: ***SerDes Line Rates (Standard Mode/Ethernet Mode)***

Width at Parallel Ports	Speed Grade			Units
	3	2	1	
128 bits	106.25			Gbps
64 bits	53.125			Gbps
32 bits	26.56			Gbps
16 bits	13.28			Gbps

SerDes (Raw Mode)

SerDes data/clock at parallel ports bypass the Ethernet/PCS controller and go to fabric core directly.

Table 16: ***SerDes Maximum Clock Rates (Raw Mode)***

Clock	Description	Speed Grade			Units
		3	2	1	
tx_block_clk	SerDes TX clock at the parallel ports	515.63			MHz
rx_block_clk	SerDes RX clock at the parallel ports	515.63			MHz
ck_tx_quad	PCS clock for SerDes quad	515.63			MHz
ck_tx_block	PCS clock for SerDes block	515.63			MHz

Table 17: ***SerDes Line Rates (Raw Mode)***

Width at Parallel Ports	Speed Grade			Units
	3	2	1	
128 bits	66			Gbps
64 bits	33			Gbps
32 bits	16.5			Gbps
16 bits	–	–	10.3125	Gbps

Ethernet

Table 18: ***Ethernet Maximum Clock Rates***

Clock	Description	Speed Grade			Units
		3	2	1	
ref_clk	Ethernet reference clock	900			MHz
ff_clk	Ethernet FIFO clock	782			MHz

Table 19: ***Ethernet Line Rates***

Width at Parallel Ports	Speed Grade			Units
	3	2	1	

Width at Parallel Ports	Speed Grade	Units
64 bits	53.125	Gbps
128 bits	106.25	Gbps

DDR4

Table 20: ***DDR4 Maximum Clock Rates***

Clock	Description	Speed Grade			Units
		3	2	1	
ddr4_clk	Controller Reference Clock	800			MHz
ddr4_clk	NoC AXI-256 Clock	800			MHz
ddr4_fabric_clk	DCI AXI-512 Clock	400			MHz

Table 21: ***DDR4 Line Rate***

Width at Parallel Ports	Rank	Speed Grade			Units
		3	2	1	
64 bits (per data pin)	1	3200			Mbps
64 bits (per data pin)	2	2400			Mbps
64 bits (per data pin)	4	1600			Mbps

GDDR6

Table 22: ***GDDR6 Maximum Clock Rates***

Clock	Description	Speed Grade			Units
		3	2	1	
gddr6_clk	Controller Reference Clock	1000			MHz
gddr6_clk	NoC AXI-256 Clock	1000			MHz
gddr6_fabric_clk	DCI AXI-512 Clock	500			MHz

Table 23: ***GDDR6 Line Rate***

Width at Parallel Ports	Speed Grades			Units
	3	2	1	
32 bits (per data pin)	16			Gbps

PCIe x8 (PCIE_0)

Table 24: ***PCIe ×8 Maximum Clock Rates***

Clock	Description	Speed Grade			Units
		3	2	1	
core_clk (pipe_clk)	Recovered clock, max is 1GHz for PCIe Gen5	1000			MHz
pcie_clk	NoC AXI-512 Clock	1000			MHz

Table 25: ***PCIe ×8 Other Specifications***

Item	Value	Units
Number of lanes supported	×1, ×4, ×8	–
Maximum link speed (per lane)	32 (Gen5)	GT/s

PCIe x16 (PCIE_1)

Table 26: ***PCIe ×16 Maximum Clock Rates***

Clock	Description	Speed Grade			Units
		3	2	1	
core_clk (pipe_clk)	Recovered clock, max is 1000 MHz for PCIe Gen5	1000			MHz
pcie_clk	NoC AXI-512 Clock	1000			MHz
pcie_express_1_master(slave)_clk	DCI AXI-512 Clock (supported for Gen1-Gen4)	500			MHz

Table 27: ***PCIe ×8 Other Specifications***

Item	Value	Units
Number of lanes supported	×1, ×4, ×8, ×16	–
Maximum link speed (per lane)	32 (Gen5)	GT/s

Chapter - 9: Speedster7t FPGA Power Rails, Speed Grades and Ordering Information

Speedster7t Power Supplies

Table 28: ***Speedster7t Power Supply Requirements***

Pin Name				
Description	**Min Voltage (V)**	**Typ Voltage (V)**	**Max Voltage (V)**	**AC Ripple (mV pk-pk)**
VCC				
Digital supply for the GDDR6 controller, DDR4 PHY and controller, Achronix PCS and the eFuse module	0.84	0.85	0.86	17
VSS				
Ground		0		
TS_VDDA				
Analog power supply to the temperature sensor	1.78	1.8	1.82	36
CLKIO_[NE/NW/SE/SW]_VDDIO				
Analog supply for clock I/O	1.46	1.5	1.61	30
	1.75	1.8	1.93	30
CLKIO_[NE/NW/SE/SW]_VREF				
Reference voltage supply for the CLKIO	0.73	0.75	0.8	15
	0.87	0.9	0.96	15
CORE_VDD				
Power supply for the FPGA fabric based on the selected speed grade.	Speed grade 1 – 0.90V			
	0.89	0.90	0.91	36
	Speed grade 2 – 0.85V			
	0.84	0.85	0.86	34
	Speed grade 3 – 0.75V			
	0.74	0.75	0.76	30

Pin Name				
DDR4_S0_VAA				
Analog supply for the DDR PLL	1.78	1.8	1.82	36
DDR4_S0_VDDQ				
I/O domain power supply for the DDR4 PHY	1.16	1.2	1.24	38
ENOC_[N/NE/NW/S/SE/SW]_PLL_VDDA				
Analog supply for the NoC PLLs	1.78	1.8	1.82	36
ENOC_[N/NE/NW/S/SE/SW]_PLL_VSSA				
Ground power supply for the NoC PLLs		0		
FUSE_VDD2				
Analog supply for the eFUSE module	1.78	1.8	1.82	36
FCU_VDDIO				
Analog supply for the GPIO associated with FCU/JTAG	1.78	1.8	1.82	36
GCG_[NE/NW/SE/SW]_PLL_VDDA				
Analog supply for the clock generator PLLs	1.78	1.8	1.82	36
GCG_[NE/NW/SE/SW]_PLL_VSSA				
Ground power supply for the Clock Generator PLLs		0		
GDDR6_[E/W]_VDDR				
Digital supply for GDDR6 PHY. This supply is used for level shifting input signals from VDDR to VDDA domain and all output signals from VDDA to VDDR domain.	0.83	0.85	0.88	34
GDDR6_[E/W]_VDDA				
Analog power supply for GDDR6 PHY. This supply is used for digital logic, custom digital, data pipes and receive delay lines. Also used as analog circuit supply, clocking, global and local clock trees.	0.83	0.85	0.87	26
GDDR6_[E/W]_VDDIO				
GDDR6 I/O power supply	1.32	1.35	1.38	27
GDDR6_[E/W]_VDDP				
PLL supply for GDDR6 PHY	1.32	1.35	1.38	27
SRDS_N_PA_VDDH				
SerDes analog high-power supply	1.16	1.2	1.3	10
SRDS_N_PA_VDDL				

Pin Name				
SerDes analog low-power supply	0.73	0.75	0.81	10
SRDS_N_PA_VSS				
SerDes ground		0		
GPIO_[N0/S0]_VDDIO				
Analog supply for the GPIO	1.07	1.1	1.14	30
	1.16	1.2	1.24	40
	1.31	1.35	1.4	50
	1.45	1.5	1.55	60
	1.75	1.8	1.86	100
GPIO_[N0/S0]_VREF				
Reference voltage supply for the GPIO	0.53	0.55	0.57	15
	0.58	0.6	0.62	20
	0.65	0.675	0.7	25
	0.73	0.75	0.78	30
	0.87	0.9	0.93	50

Speedster7t Speed Grades

Table 29: *Speedster7t Speed Grades*

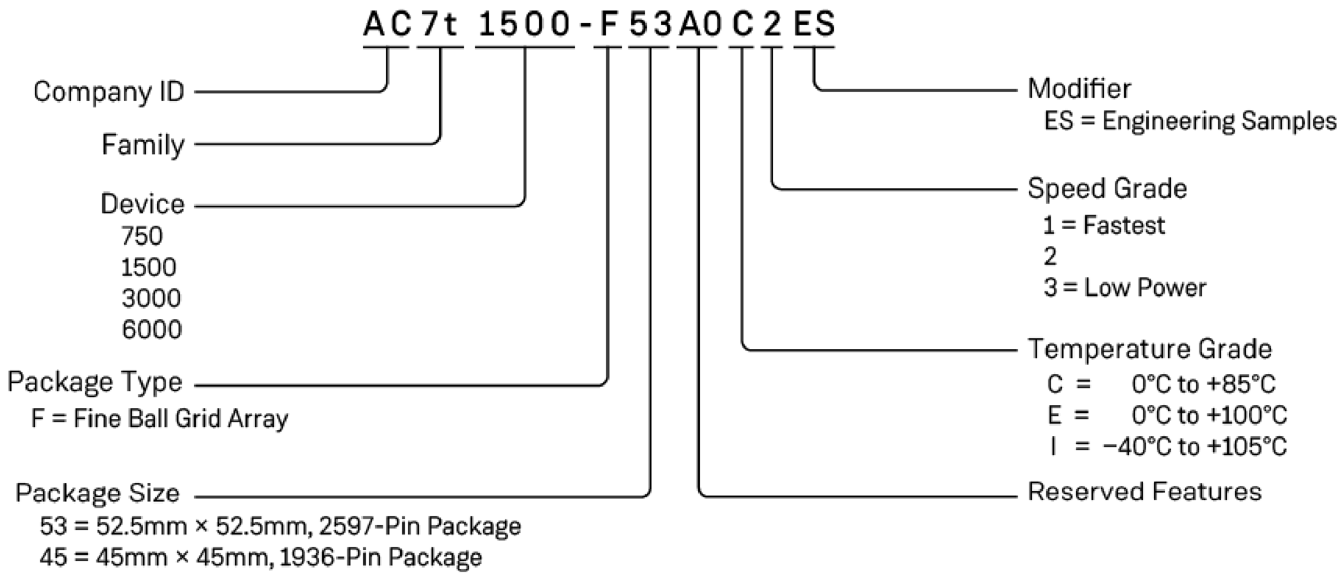
Speed Grade	Nominal Voltage (V)	Relative Performance
1	0.90	1.6×
2	0.85	1.3×
3	0.75	1.0×

Speedster7t Lifetime and Temperature Ranges

Achronix Speedster7t devices have an operating lifetime of ten years and can support the following temperature grades:

- Commercial (0°C to +85°C)
- Extended (0°C to +100°C)
- Industrial (−40°C to +105°C)

Speedster7t Ordering Codes



Revision History

The following table lists the revision history of this document.

Version	Date	Description
1.0	24 Mar 2020	• Initial release.

1.1	12 Jun 2020	• Updated number of special-purpose I/O (SPIO) in table, Speedster7t FPGA Family Features Table (see page 9).
		• Added new sections:
		  • Special-Purpose I/O (SPIO) (see page 22)
		  • Speedster7t FPGA Timing Data (see page 39)