Speedster22i™ FPGA Family Power Estimator Tool User Guide

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1 Power Estimator overview

The Achronix Power Estimator tool provides a platform to calculate the power requirements for Achronix Speedster 22i device families. This user guide gives a detailed overview of the various power components depending on the utilization of various components in the design. The power estimator tool can be used at any stage of the FPGA design to get an estimate of the total power dissipation from the device. It comes in handy to get a first hand estimate of the power specification at the start of the design so the design utilization can be altered based on the power requirements. This estimate could then be compared with post-implementation results for comparison purposes.

The Achronix Power Estimator is a spreadsheet that takes various parameters as inputs from the user to estimate the total power dissipated. This includes device characteristics, thermal characteristics and utilization of various components like BRAMs, LRAMs, I/Os, LUTs, Clocks and Hard IPs. To get a good estimate of the design's power profile, the user is required to enter a more realistic estimate of the design utilization.

2 System requirements and setup

- The Achronix Power Estimator tool is compatible with Microsoft Excel 2007
- For efficient functioning of the tool, macros should be enabled. By default, the security setting has macros disabled. This setting can be changed by enabling it in the Trust Center
    - Click the **Microsoft Office Button**  , and then click **Excel Options**.
    - Click **Trust Center**, click **Trust Center Settings**, and then click **Macro Settings**.
    - Enable macros

3 Power Estimator Worksheets

3.1 Power Central Worksheet

The Power Central worksheet is the main worksheet of the tool where the breakdown of various power dissipation components is displayed. It is split into four parts: System variables, Power usage in Watts, Current by power supply, Power usage summary

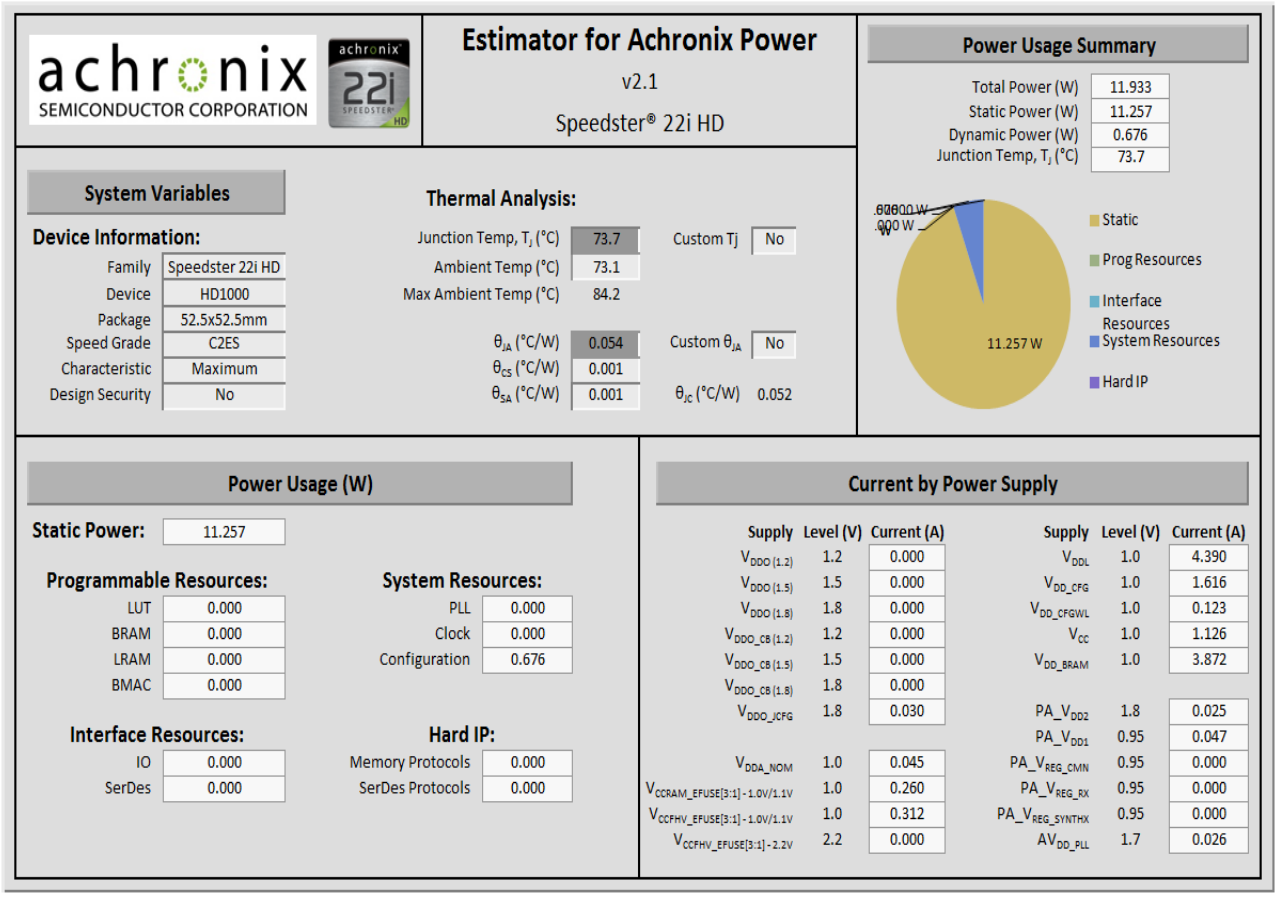


Figure 3-1 Power Central Worksheet

3.1.1 System variables

This part includes two sections which are the Device information and Thermal Analysis

3.1.1.1 Device information

The Device information takes in the following input parameters to calculate power

Table 3-1 System variables input parameters

Parameter	Description
Family	Achronix device for which power estimation need to be calculated
Device	Type of Speedster device : HD680/HD1000
Package	Type of package used : 45x45 mm / 52.5x52.5 mm
Speed Grade	This option allows the user to select the desired speed grade for the target device: C2ES/C3ES C2 offers fastest speed grade for HD1000 under normal conditions
Characteristic	This option allows the user to select the device characteristics used for static power calculation: Typical – This is the average (50%) power dissipation characteristics used for static power calculation. Maximum – Worst case device characteristics used for static power calculation. In order to account for worst-case process variation, it is recommended to set the characteristics to **Maximum**
Design security	This option allows the user to enable or disable design security feature i.e if the application requires fuse blowing (eg. programming encryption fuses for design security)

3.1.1.2 Thermal Analysis

The following input parameters are present for user selection

Table 3-2 Thermal Analysis input parameters

Parameter	Description
Junction Temperature, T_J(^{o}C)	The junction temperature or operating temperature refers to the temperature of the silicon die within the package of the device when the device is powered. $T_J = T_A + (P \times \theta_{JA})$ where T_J is the Junction temperature in ^{o}C T_A is the Ambient temperature in ^{o}C P is the total power dissipated in Watts θ_{JA} is the Junction-to-ambient thermal resistance in ^{o}C/W
Custom T_J	Allows the user to enable/disable user-defined T_J When custom T_J is disabled, the junction temperature is calculated based on the formula above and when enabled, the user has the choice to enter a value.
Ambient temperature, (^{o}C)	The ambient temperature refers to the temperature of the surrounding environment (typically air) when the device is powered
Max Ambient temperature, (^{o}C)	The maximum ambient temperature should be such that the junction temperature does not exceed 85^{o}C. Achronix devices support temperature range from 25 ^{o}C -85^{o}C
θ_{JA} (°C/W)	Junction-to-ambient thermal resistance $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$
θ_{JC}(°C/W)	Junction-to-case thermal resistance
θ_{CS}(°C/W)	Case-to-heat sink thermal resistance
θ_{SA}(°C/W)	Heat sink-to-ambient thermal resistance
Custom θ_{JA}	This option when enabled, allows the user to enter a value for θ_{JA} keeping the other thermal resistance values unchangeable When disabled, the user may enter values for θ_{CS} and θ_{SA} and θ_{JA} is calculated accordingly

3.1.2 Power Usage

3.1.2.1 Power Dissipation in FPGA

The total power dissipated comprises two components; the static power and the dynamic power. Static power or standby power is the power dissipated when the device is in an unconfigured state after power-up. It depends on several factors including temperature, leakage current and operating voltages.

Dynamic or switching power dissipation is caused by switching activity inside FPGA and at I/O interfaces and is a function of switching frequency, operating voltage and capacitance. A higher operating frequency leads to more signal transitions thereby increasing dynamic power dissipation.

The power usage section gives a breakdown of the different power dissipation sources that contribute to static and dynamic power. These include

Static Power

The total static power value depends on the device and thermal characteristics. The maximum static power is 15W at 85 ^{o}C junction temperature for maximum (worst-case) device characteristic.

Dynamic Power

The remaining section in Power usage contributes towards dynamic power. The total dynamic power is a sum of all the following resources and Hard IPs

3.1.2.2 Programmable resources

This section summarizes the power dissipated by the total LUTs, BRAMs, LRAMs and BMACs in the device. Each of these components has a separate worksheet for power calculation which will be explained in detail later in this document.

3.1.2.3 Interface resources

This section includes power dissipated by I/O and SerDes interfaces in the device. Each of these components has a separate worksheet for power calculation which will be explained in detail later in this document.

3.1.2.4 System resources

This includes power dissipated by the total PLLs and clocks used in the design and also the configuration power. The configuration power is the total power consumed from initial power up to stepping into user mode. The steps are illustrated in Table 3-1

Table 3-1 Power-up and Configuration Sequencing steps

1	2	3	4	5	6	7	8
Device power-up	Read non-volatile memories	Clear configuration memory	Bitstream sync and device ID	Load configuration bits	CRC check	Startup sequence	User mode

The configuration power for Achronix HD1000 device is set at 0.676 W

3.1.2.5 Hard IP

This section lists the power consumed by the hard IPs used in the design. They are split into the following protocols accordingly.

Memory Protocols: This section includes the power consumed by the DDR controller Hard IP

SerDes Protocols: This section includes the power consumed by the other Hard IPs like 10G/40G/100G Ethernet, Interlaken and PCI Express

A more detailed review of the Hard IPs will be addressed in the Hard IP worksheet later in this document. Fig 3-2 shows the Power Usage section in the Power Central worksheet

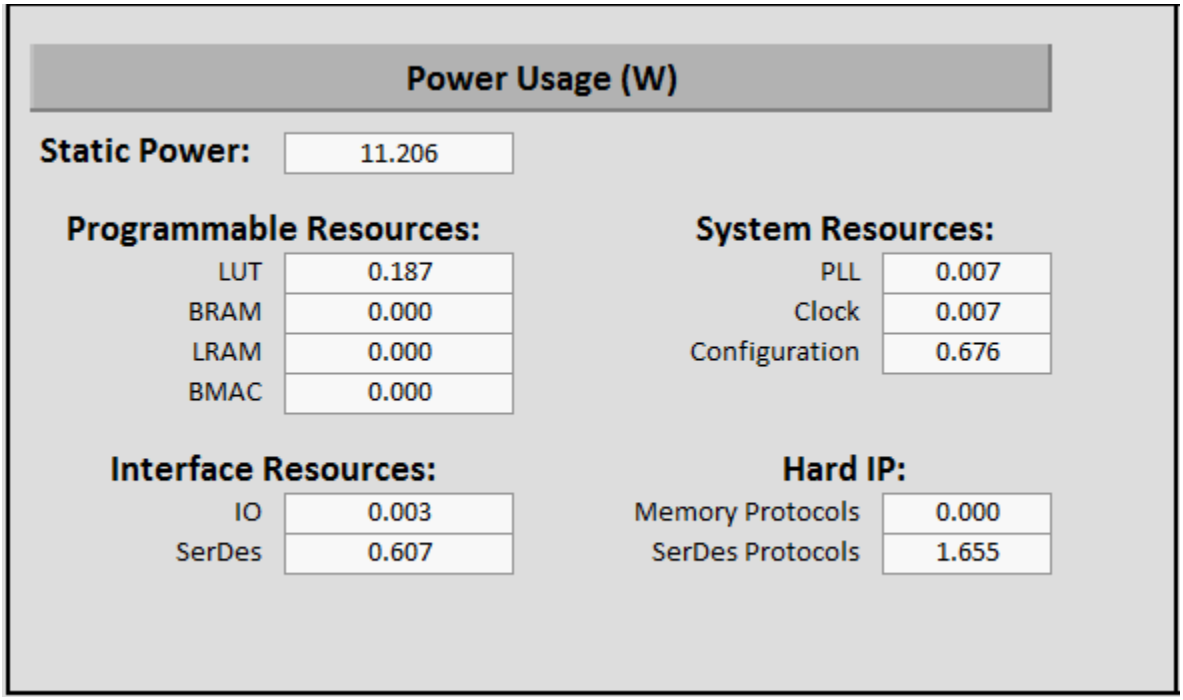


Fig 3-2 Power Usage section

3.1.3 Power Usage Summary

This section provides a summary of all the power dissipation components like the Total Power (W), Static Power (W) and Dynamic Power (W). It also provides a pie diagram of the different power components. Fig 3-3 shows a list of power components and the associated pie diagram.

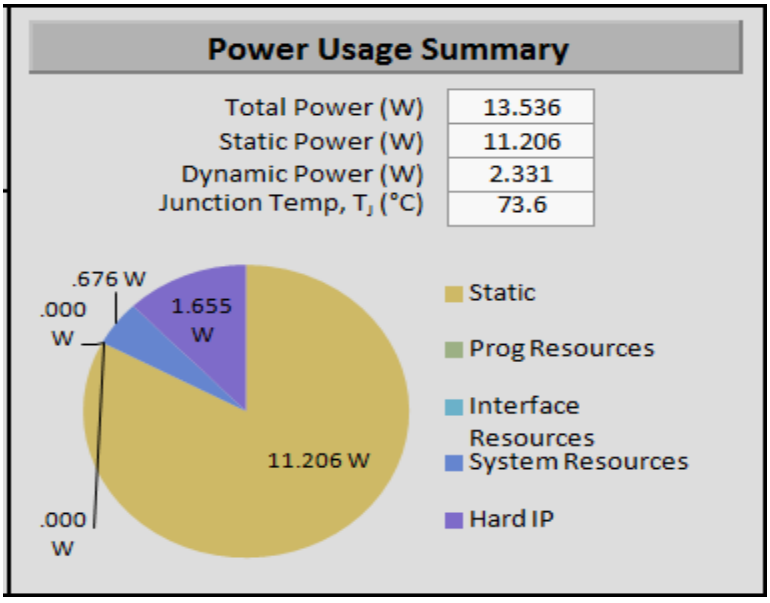


Fig. 3-3 Power Usage Summary

3.1.4 Current by Power Supply

This section lists the various Supply voltages and the associated current in the fabric. Fig 3-4 shows the current by power supply section in the Power Central worksheet and Table 3-2 describes the various voltage supplies used in power calculation

Current by Power Supply

Supply	Level (V)	Current (A)	Supply	Level (V)	Current (A)
$V_{DDO\ (1.2)}$	1.2	0.000	V_{DDL}	1.0	4.370
$V_{DDO\ (1.5)}$	1.5	0.000	V_{DD_CFG}	1.0	1.609
$V_{DDO\ (1.8)}$	1.8	0.000	V_{DD_CFGWL}	1.0	0.122
$V_{DDO\_CB\ (1.2)}$	1.2	0.000	V_{CC}	1.0	2.775
$V_{DDO\_CB\ (1.5)}$	1.5	0.000	V_{DD_BRAM}	1.0	3.855
$V_{DDO\_CB\ (1.8)}$	1.8	0.000			
V_{DDO_JCFG}	1.8	0.030	PA_V_{DD2}	1.8	0.025
			PA_V_{DD1}	0.95	0.047
V_{DDA_NOM}	1.0	0.045	$PA\_V_{REG\_CMN}$	0.95	0.000
$V_{CCRAM\_EFUSE[3:1]\ -\ 1.0V/1.1V}$	1.0	0.260	$PA\_V_{REG\_RX}$	0.95	0.000
$V_{CCFHV\_EFUSE[3:1]\ -\ 1.0V/1.1V}$	1.0	0.312	$PA\_V_{REG\_SYNTHX}$	0.95	0.000
$V_{CCFHV\_EFUSE[3:1]\ -\ 2.2V}$	2.2	0.000	AV_{DD_PLL}	1.7	0.026

Fig. 3-4 Current by Power supply

Table 3-2 Voltage Supplies Used In Power Calculation

Parameter	Description
VDDL	Power supply for FPGA core
VDD_CFG	Supply voltage for the configuration memory SRAM cells in the FPGA fabric
VDD_CFGWL	Power Supply for the word lines of the configuration memory SRAM cells in the FPGA fabric
VCC	Digital Power Supply for FPGA circuitry in the I/O ring, including the Hard IP
VDD_BRAM	Power Supply for Block RAMS in Fabric including BRAM internal circuitry like write/read timers, address decoders, sense amplifiers etc.
PA_VDD2	SerDes Analog High Power Supply
PA_VDD1	SerDes Analog Low Power Supply
PA_VREG_CMN	SerDes Regulator Power Supply
PA_VREG_RX	SerDes Regulator Power Supply
PA_VREG_SYNTHX	SerDes Regulator Power Supply
AVDD_PLL	Analog power supply for the PLLs feeding the FPGA core fabric.
VDDO	Bank I/O supply voltage
VDDO_CB	Power Clock bank I/O supply voltage
VDDO_JCFG	Supply voltage powering the I/O buffers for the IEEE 1149.1 JTAG interface
VDDA_NOM	Analog Power Supply for FPGA circuitry in the I/O ring
VCCRAM_EFUSE	Efuse Power Supply normal / read operations
VCCFHV_EFUSE	Efuse Power Supply for Fuse Program / Erase operations

More details on these power supplies can be found in http://www.achronix.com/wp-content/uploads/docs/Speedster22i_PinConnections_PowerSequencing_User_Guide_UG042.pdf

3.2 LUT Worksheet

The LUT power worksheet summarizes the percentage of the total available LUT utilization and dynamic power estimation for the total LUTs used in the design

It also contains a section to enter the values of the following parameters on the LUT usage in the design

- Function
- LUT count
- FF count
- Clock (MHz)
- Toggle rate
- Fanout
- Power (W)

LUT Power

Device Utilization:			Dynamic Power Summary	
Device:	HD1000		LUT Power (W):	0.000
Available LUTs / FFs:	700,000		% of Total Dynamic:	0.00%
Used LUTs:	0	0%		
Used FFs:	0	0%		

Function	LUT Count	FF Count	Clock (MHz)	Toggle Rate	Fanout	Power (W)
	0	0	100	12.5%	Medium	0.000
				12.5%	Medium	0.000
				12.5%	Medium	0.000
				12.5%	Medium	0.000
				12.5%	Medium	0.000
				12.5%	Medium	0.000
				12.5%	Medium	0.000

Fig 3-5 LUT Worksheet

Table 3-3 Input Parameters on LUT Power worksheet

Input parameter	Description
Function	Description about the functionality/module associated with the LUT. This entry is optional
LUT count	The number of LUT used in the function/module of the design
FF count	The total flipflop count used with the LUTs
Clock (MHz)	The maximum clock frequency that is driving the logic
Toggle rate	The percentage at which the logic toggles on each clock cycle
Fanout	The average number of blocks that will be driven by the LUTs and flipflops. The value ranges from very low, low, medium to high and very high.
Power (W)	This column calculates the total power use by the LUTs and flipflops and its contribution towards the total dynamic power percentage which will be reflected in the Power Central worksheet

3.3 BRAM worksheet

The BRAM Power worksheet summarizes the total BRAM percentage used versus the available BRAMs and the total dynamic power dissipation percentage depending on the values entered on the following input parameters. It also displays the voltage supply and current flow as a result of BRAM utilization.

VDDL supply is used to power some of the peripheral circuitry used to help interface BRAM with surrounding circuitry and routing

VDD_BRAM supply is used to power BRAM internal circuitry like write/read timers, address decoders, sense amplifiers etc.

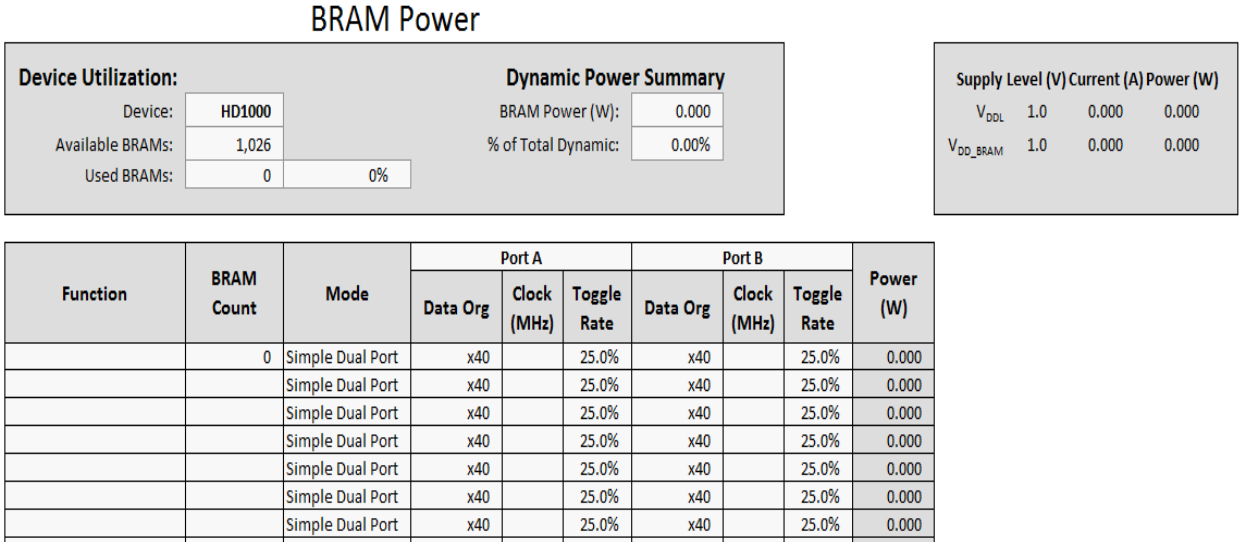


Fig 3-6 BRAM Worksheet

Table 3-4 Input Parameters on BRAM Power worksheet

Input parameter	Description
Function	Description about the functionality/module associated with the BRAM. This entry is optional
BRAM count	The number of BRAM used in the function/module of the design
Mode	BRAM mode of operation: ROM/Single port/Simple dual port/True dual port A single-port RAM has one port with a read and write control signal. A simple dual-port RAM has one read port and one write port. A true dual-port RAM has two ports, each with a read and write control signal. ROMs are read-only single-port RAMs
Data Org	The data width of BRAMs for Port A and Port B. The values range from x1 to x40
Clock (MHz)	The maximum clock frequency that is driving the BRAMs at Port A and Port B. Port B is ignored in case of single port or ROM based BRAMs
Toggle rate	The percentage at which the logic toggles on each clock cycle on Port A and Port B.
Power (W)	This column calculates the total power use by the BRAMs and its contribution towards the total dynamic power percentage which will be reflected in the Power Central worksheet

3.4 LRAM worksheet

The LRAM Power worksheet summarizes the total LRAM percentage used versus the available LRAMs and the total dynamic power dissipation percentage depending on the values entered on the following input parameters

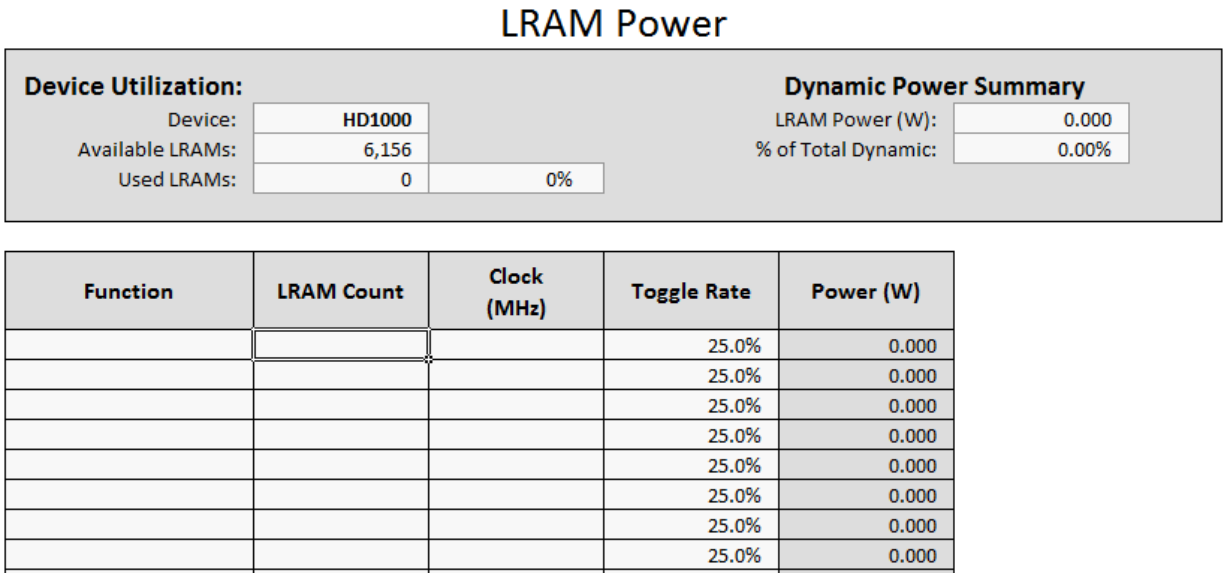


Fig 3-7 LRAM Worksheet

Table 3-5 Input Parameters on LRAM Power worksheet

Input parameter	Description
Function	Description about the functionality/module associated with the LRAM. This entry is optional
LRAM count	The number of LRAM used in the function/module of the design
Clock (MHz)	The maximum clock frequency that is driving the LRAMs
Toggle rate	The percentage at which the logic toggles on each clock cycle
Power (W)	This column calculates the total power use by the BRAMs and its contribution towards the total dynamic power percentage which will be reflected in the Power Central worksheet

3.5 BMAC worksheet

The BMAC Power worksheet summarizes the total BMAC percentage used versus the available BMACs and the total dynamic power dissipation percentage depending on the values entered on the following input parameters

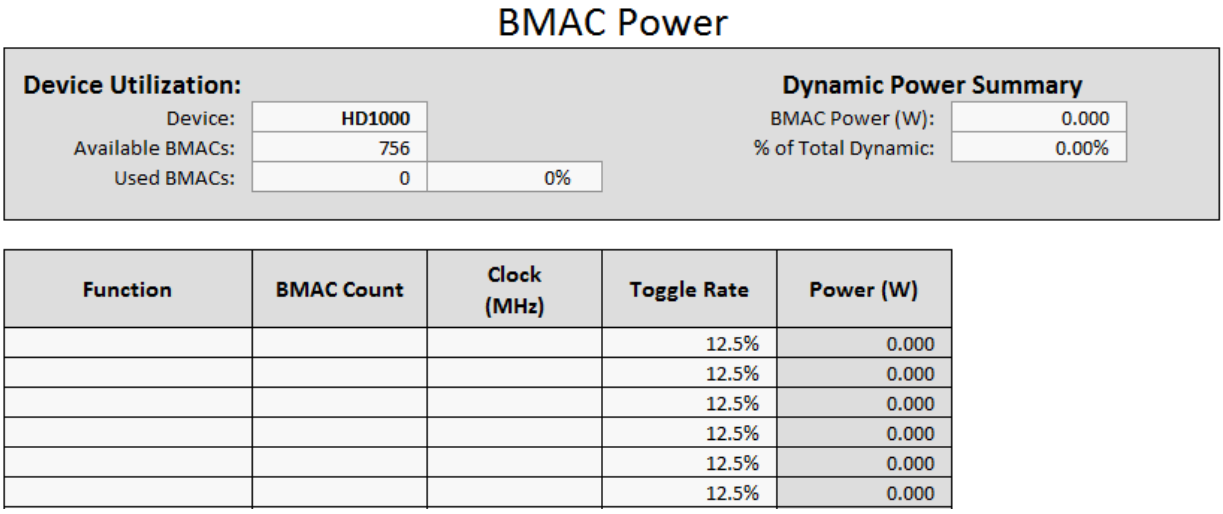


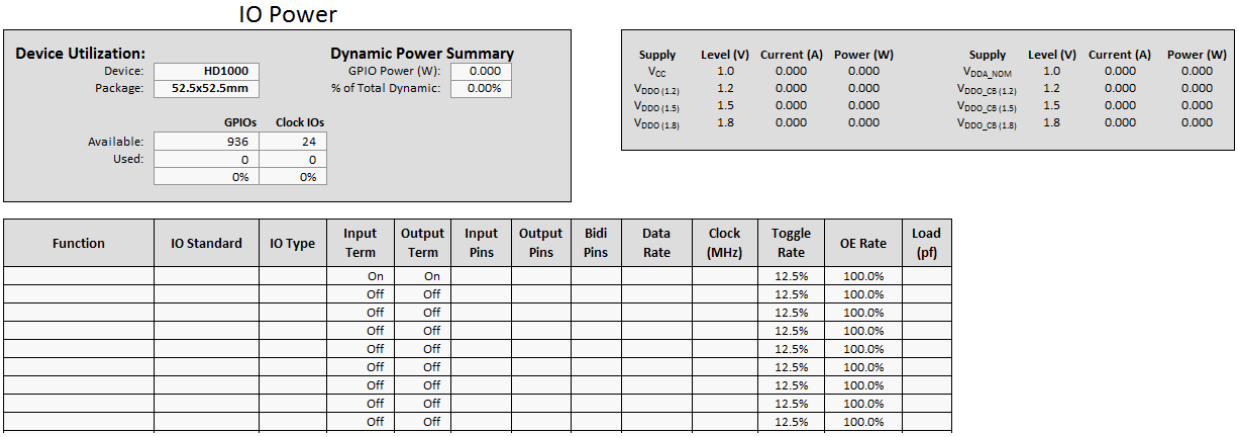
Fig 3-8 BMAC Worksheet

Table 3-6 Input Parameters on BMAC Power worksheet

Input parameter	Description
Function	Description about the functionality/module associated with the BMAC. This entry is optional
BMAC count	The number of BMAC used in the function/module of the design
Clock (MHz)	The maximum clock frequency that is driving the BMACs
Toggle rate	The percentage at which the logic toggles on each clock cycle
Power (W)	This column calculates the total power use by the BMACs and its contribution towards the total dynamic power percentage which will be reflected in the Power Central worksheet

3.6 I/O worksheet

The I/O Power worksheet summarizes the total I/O percentage used versus the available I/Os and the total dynamic power dissipation percentage depending on the values entered on the following input parameters. It also displays the voltage supply and current flow as a result of I/O utilization.



IO Power

Device Utilization:

Device:	HD1000
Package:	52.5x52.5mm

Dynamic Power Summary

GPIO Power (W):	0.000
% of Total Dynamic:	0.00%

	GPIOs	Clock IOs
Available:	936	24
Used:	0	0
	0%	0%

Supply	Level (V)	Current (A)	Power (W)	Supply	Level (V)	Current (A)	Power (W)
V_{CC}	1.0	0.000	0.000	V_{DDA_NOM}	1.0	0.000	0.000
$V_{DDO\ (1.2)}$	1.2	0.000	0.000	$V_{DDO\_CB\ (1.2)}$	1.2	0.000	0.000
$V_{DDO\ (1.5)}$	1.5	0.000	0.000	$V_{DDO\_CB\ (1.5)}$	1.5	0.000	0.000
$V_{DDO\ (1.8)}$	1.8	0.000	0.000	$V_{DDO\_CB\ (1.8)}$	1.8	0.000	0.000

Function	IO Standard	IO Type	Input Term	Output Term	Input Pins	Output Pins	Bidi Pins	Data Rate	Clock (MHz)	Toggle Rate	OE Rate	Load (pf)
			On	On						12.5%	100.0%	
			Off	Off						12.5%	100.0%	
			Off	Off						12.5%	100.0%	
			Off	Off						12.5%	100.0%	
			Off	Off						12.5%	100.0%	
			Off	Off						12.5%	100.0%	
			Off	Off						12.5%	100.0%	
			Off	Off						12.5%	100.0%	
			Off	Off						12.5%	100.0%	

Fig 3-9 I/O Worksheet

Table 3-7 Input Parameters on I/O Power worksheet

Input Parameter	Description
Function	Description about the functionality/module associated with the I/Os. This entry is optional
I/O standard	Selection of industry standard I/O used for the I/Os. The dynamic power varies with the selection of I/O standard
I/O type	Type of I/O used: GPI/O/Clock I/O
Input termination	Option to select if input termination is used or not
Output termination	Option to select if output termination is used or not
Input pins	Total number of I/Os used as input pins
Output pins	Total number of I/Os used as output pins
Bidirectional pins	Total number of I/Os used as bidirectional pins
Data rate	Option to choose between Single Data rate or Double Data Rate
Clock (MHz)	The maximum clock frequency at which the I/Os are toggling
Toggle rate	The percentage at which the I/Os toggle on each clock cycle

OE rate	The percentage of time for which the output I/O pins is enabled and bidirectional I/O pins are output pins and enabled. The time for which OE is disabled, the bidirectional I/Os are inputs and output I/O pins are tristated
Load (pF)	The value of I/O pin capacitance loading

3.7 SerDes worksheet

The SerDes Power worksheet summarizes the total SerDes percentage used I/Os and the total dynamic power dissipation percentage depending on the values entered on the following input parameters. It also displays the voltage supply and current flow as a result of SerDes utilization.

PA_V_{DD1}, PA_V_{DD2}, $PA\_V_{REG\_CMIN}$, $PA\_V_{REG\_RX}$ and $PA\_V_{REG\_SYNTHX}$ are used to power the PMA and V_{CC} power supply is used to power PCS of SerDes.

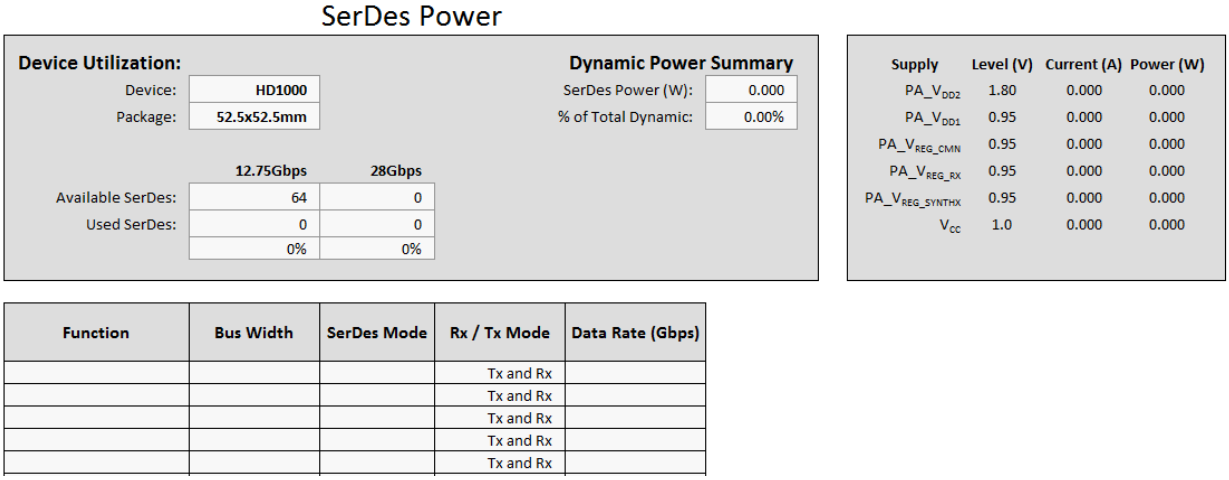


Fig 3-10 SerDes Worksheet

Table 3-8 Input Parameters on SerDes Power worksheet

Input Parameter	Description
Function	Description about the functionality/module associated with the SerDes. This entry is optional
Bus Width	Defines the number of data bits used by the SerDes interface
SerDes mode	SerDes operation mode: 12.75 Gbps/28 Gbps *Note: 28 Gbps SerDes will no longer be supported in Speedster22i HD family*

Rx/Tx mode	Defines whether the Serdes would be used in Tx mode or Rx mode or both Tx and Rx
Data Rate (Gbps)	Desired transmit and receive data rates for SerDes. The data rate must be between 1.0625 Gbps and 12.75 Gbps

3.8 PLL Worksheet

The PLL Power worksheet summarizes the total PLL percentage used of the 16 available PLLs and the total dynamic power dissipation percentage depending on the values entered on the following input parameters.

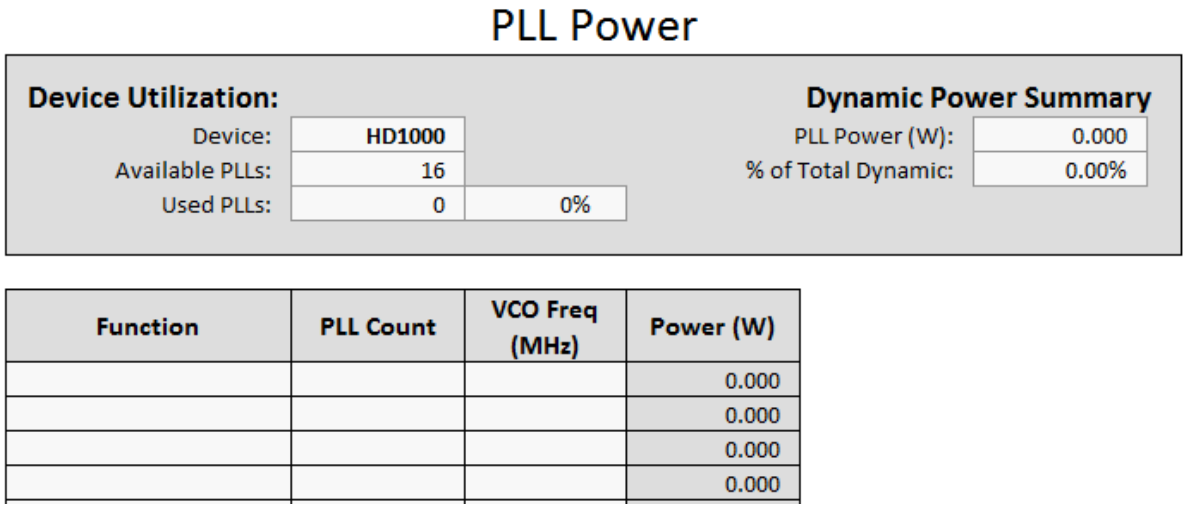


Fig 3-11 PLL Worksheet

Table 3-9 Input Parameters on PLL Power worksheet

Input Parameter	Description
Function	Description about the functionality/module associated with the PLLs. This entry is optional
PLL count	Total PLL count used
VCO Frequency (MHz)	VCO output frequency. Allowed range is between 1250 MHz and 2500 MHz

3.9 Clock Worksheet

The Clock Power worksheet summarizes the total dynamic power dissipation percentage depending on the values entered on the following input parameters.

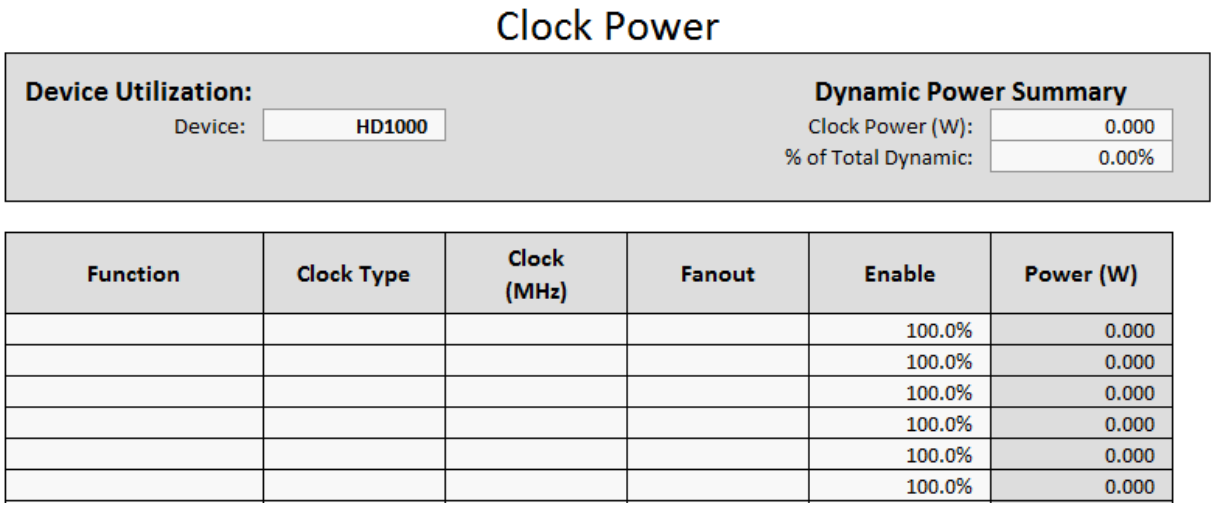


Fig 3-12 Clock Worksheet

Table 3-10 Input Parameters on Clock Power worksheet

Input Parameter	Description
Function	Description about the functionality/module associated with the clocks. This entry is optional
Clock type	Defines whether the clock used is a direct or global clock
Clock (MHz)	Clock output frequency
Fanout	The total fanout from the output of clock network to all registers including LUTs, BRAMs, LRAMs and MACs
Enable	The percentage of time for which the clock tree is enabled

3.10 Hard IP Worksheet

The Hard IP Power worksheet summarizes the total hard IP percentage used of the available IPs and the total dynamic power dissipation percentage depending on the values entered on the following input parameters.

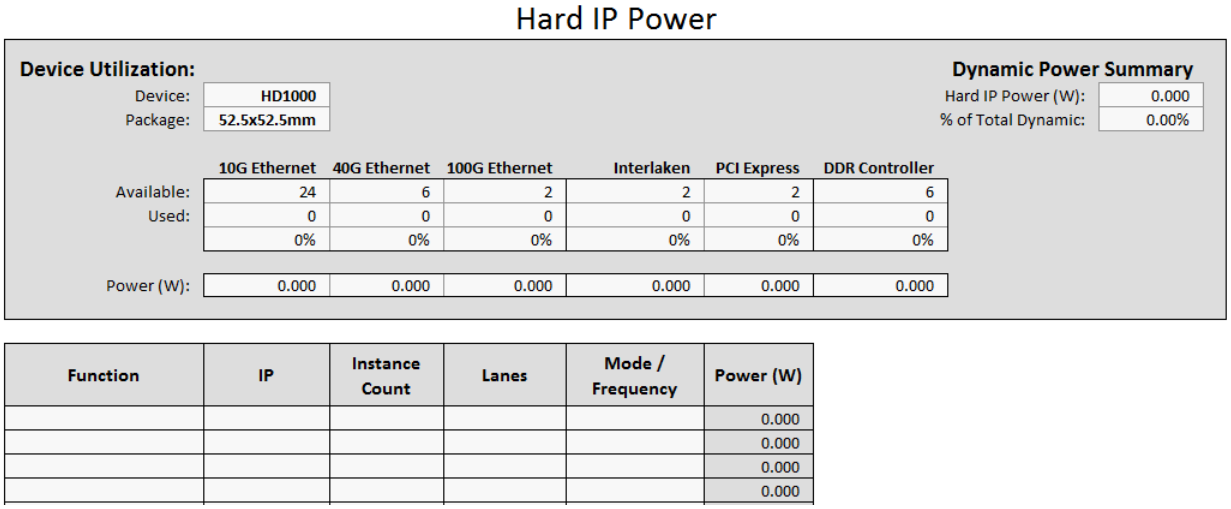


Fig 3-13 Hard IP Worksheet

Table 3-11 Input Parameters on Hard IP Power worksheet

Input Parameter	Description
Function	Description about the functionality/module associated with the hard IP. This entry is optional
IP	Defines the IP used : 10G/40G/100G Ethernet/Interlaken/PCI Express/ DDR Controller
Instance count	The total number of instances for each IP
Lanes	The total number of lanes for each IP. The allowed number of lanes vary with the selection of the IP
Mode/Frequency	The mode/frequency at which the Hard IP operates

4 Release History

Date	Version	Comments
7/28/2015	1.0	Initial Achronix release