Speedster22i Pin Connections and Power Supply Sequencing User Guide

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Pin Connection Guidelines

Please see the table below on guidelines for connecting all IOs on the Speedster22i HD FPGAs. For completeness, debug I/Os that have no user functionality have also been included and are indicated by a grey background.

Pin Name	Pin Group	Type	Description	Connection Guidelines
12.75 Gbps SerDes (64 lanes)				
PAD_TE_I_BCK_REF_P/M_LNUM[31:0]	N12P75G	Clock	The 12.75 Gbps SerDes reference clock supplied from either a single-ended or differential external source. There is 1 differential pair for each of 2, 12.75Gbps lane.	Connect these clocks for all SerDes lanes used in the interface. Unused clocks should be tied to their own individual GND via an optional 50Ω +/- 1% termination resistor. ***Note: For PCIe Gen3 operation when using the hard PCIe controller, reference clocks for all 8 SerDes lanes need to be connected regardless of the data width implemented.***
PAD_TE_I_BA_RX_P/M_LNUM[31:0]	N12P75G	Input	Receive differential inputs to the 12.75 Gbps SerDes. One pair for each lane.	Connect unused receive pins to GND via an optional 50Ω +/- 1% termination resistor.
PAD_TE_O_BA_APROBE_LNUM[31:0]	N12P75G	Output	The 12.75 Gbps SerDes Analog DC test pad used internally for debug and testing, one for each lane.	Leave unconnected.
PAD_TE_O_BA_TX_P/M_LNUM[31:0]	N12P75G	Output	Transmit differential outputs from the 12.75 Gbps SerDes. There is one differential pair per each 12.75Gbps lane.	These pins should be AC coupled. Leave all unused transmit pins unconnected.
PAD_BE_I_BCK_REF_P/M_LNUM[31:0]	S12P75G	Clock	The 12.75 Gbps SerDes reference clock supplied from either a single-ended or differential external source. There is 1 differential pair for each of 2, 12.75Gbps lane.	Connect these clocks for all SerDes lanes used in the interface. Unused clocks should be tied to their own individual GND via an optional 50Ω +/- 1% termination resistor. ***Note: For PCIe Gen3 operation when using the hard PCIe controller, reference clocks for all 8 SerDes lanes need to be connected regardless of the data width implemented.***
PAD_BE_I_BA_RX_P/M_LNUM[31:0]	S12P75G	Input	Receive differential inputs to the 12.75 Gbps SerDes. One pair for each lane.	Connect unused receive pins to GND via an optional 50Ω +/- 1% termination resistor.
PAD_BE_O_BA_APROBE_LNUM[31:0]	S12P75G	Output	The 12.75 Gbps SerDes Analog DC test pad used for ATE and bench testing, one for each lane	Leave unconnected.
PAD_BE_O_BA_TX_P/M_LNUM[31:0]	S12P75G	Output	Transmit differential outputs from the 12.75 Gbps SerDes. There is one differential pair per each 12.75Gbps lane.	These pins should be AC coupled. Leave all unused transmit pins unconnected.

IEEE1149.1 JTAG Interface				**Do not leave JTAG I/Os unconnected. The JTAG interface should be brought out to a JTAG header on the board.**
TMS	JTAG	Input	Test Mode Select (TMS) input controlling the test access port (TAP) controller state machine transitions. This input is captured on the rising edge of the test logic clock (TCK).	This dedicated pin is equipped with an internal pull-up resistor to place the test logic in the Test-Logic-Reset state. Connect this pin using a 10-kΩ +/- 5% pull-up resistor to VDDO_JCFG (1.8V).
TCK	JTAG	Input	Dedicated test clock used to advance the TAP controller and clock in data on TDI input and out on TDO output. The maximum frequency for TCK is 6MHz.	Connect this pin using a 1-kΩ +/- 1% pull-down resistor to GND.
TDI	JTAG	Input	Serial input for instruction and test data. Data is captured on the rising edge of the test logic clock.	Dedicated pin with an internal pull-up resistor. Connect this pin using a 10-kΩ +/- 5% pull-up resistor to VDDO_JCFG (1.8V).
TRSTN	JTAG	Input	Active-low reset input used to initialize the TAP controller.	Dedicated pin and an optional port on some devices. Connect this pin using a 4.7-kΩ +/- 5% pull-down resistor to GND.
TDO	JTAG	Output	Serial output for data from the test logic. TDO is set to an inactive drive state (high impedance) when data scanning is not in progress. TDO drives out valid data on the falling edge of the TCK input.	Use a 10-kΩ +/- 5% pull-up resistor to VDDO_JCFG (1.8V) to minimize leakage in the TDI input buffer of interfacing devices.
Configuration Interface				
CONFIG_STATUS	CFG	Open drain output	Signal from open-drain output pulled low by FCU until the configuration memory is successfully cleared. After this, I/O is tri-stated and the external pull-up should pull this signal high.	It is recommended to connect this signal to an LED as an indicator on the board. In this case, use an external 10-kΩ +/- 5% pull-up resistor to 3.0V/3.3V and drive a 1-kΩ resistor to the input of a FET to turn on the LED. If LED usage is not desired, this signal can be pulled-up to 1.8V (VDDO_JCFG / PA_VDD2) using the same 10-kΩ pull-up resistor.
CONFIG_RSTN	CFG	Input	Asynchronous active-low reset input clearing the configuration memory in the device and the logic in the FPGA configuration unit (FCU).	Connect directly to the configuration controller. Pull-up/pull-down options can be done in one of two ways: 1. If the configuration controller will always be driving this input, the pin can be pulled-down to GND using a 4.7-kΩ +/- 5% resistor to ensure that the FPGA will be in a reset state on power-up. 2. If the pin may sometimes not be driven by the configuration controller or tri-stated, it Is imperative that it be pulled-up to 1.8V (VDDO_JCFG / PA_VDD2) through a 4.7-kΩ +/- 5% resistor.

<table>
<tr>
<td>CONFIG_MODESEL[2:0]</td>
<td>CFG</td>
<td>Input</td>
<td>Configuration mode selection inputs to define the FPGA configuration unit (FCU) mode of operation.

<table><tr><th>Configuration Mode</th><th>CONFIG_MODESEL[2:0]</th></tr><tr><td>Serial x1 Flash</td><td>001</td></tr><tr><td>Serial x4 Flash</td><td>010</td></tr><tr><td>CPU</td><td>100</td></tr><tr><td>JTAG</td><td>Always active</td></tr></table></td>
<td>Do not leave these pins unconnected. They should be connected to configurable inputs like DIP switches to toggle between modes of operation for debug. If this is not possible or desired, based on the config scheme, these pins should be tied to 1.8V (VDDO_JCFG / PA_VDD2) or GND.</td>
</tr>
<tr>
<td>PROGRAM_ENABLE[1:0]</td>
<td>CFG</td>
<td>Input</td>
<td>Pin enabling the programming of the eFuse for the AES encryption keys, which is done in the manufacturing and testing of the devices. These input pins will not be usable by customers.</td>
<td>Tie to GND.</td>
</tr>
<tr>
<td>CONFIG_DONE</td>
<td>CFG</td>
<td>Input with open-drain or active output</td>
<td>Pin pulled low by FCU prior to the completion of device configuration. After the device successfully completes configuration, this pin is either tri-stated or can optionally be driven high. The default behavior is open-drain, tri-stating the pin when the device is properly configured. If a device configuration error occurs, the CONFIG_DONE output will remain low. Holding this pin low on the board can be used as a method to synchronize the start-up of multiple devices.</td>
<td>In the default mode of operation, it is recommended that this signal be connected to an LED as an indicator on the board. In this case, use an external 10-kΩ +/- 5% pull-up resistor to 3.3V and drive a 1-kΩ resistor to the input of a FET to turn on the LED. If LED usage is not desired, this signal can be pulled-up to 1.8V (VDDO_JCFG / PA_VDD2) instead using the same 10-kΩ pull-up resistor.</td>
</tr>
<tr>
<td>CONFIG_CLKSEL</td>
<td>CFG</td>
<td>Input</td>
<td>Pin controlling whether the FCU clock is sourced from the TCK input or the CPU_CLK input.

<table><tr><th>CONFIG_SYS_CLK_BYPASS</th><th>CONFIG_CLKSEL</th><th>CONFIG_MODESEL [2:0]</th><th>FCU CLK</th></tr><tr><td>0</td><td>0</td><td>001, 010</td><td>On-chip oscillator</td></tr><tr><td>1</td><td>0</td><td>001, 010</td><td>CPU_CLK</td></tr><tr><td>0/1</td><td>0</td><td>100</td><td>CPU_CLK</td></tr><tr><td>0</td><td>1</td><td>000, 001, 010, 100</td><td>TCK</td></tr></table></td>
<td>Do not leave this pin unconnected. It should be connected to a configurable input like a DIP switch to toggle between modes of operation for debug. If this is not possible or desired, tie this off to 1.8V (VDDO_JCFG / PA_VDD2) or GND based on the desired clock for the configuration mode.</td>
</tr>
<tr>
<td>HOLDN</td>
<td>CFG</td>
<td>Input / Output</td>
<td>In the SPI mode of operation, the hold signal output for SPI flash devices. In CPU mode, this bit is the bidirectional data bit 5, DQ[5].</td>
<td>Connect directly to the configuration controller. Do not leave this pin unconnected.</td>
</tr>
<tr>
<td>CPU_CLK</td>
<td>CFG</td>
<td>Clock</td>
<td>Maximum 6MHz. Used as FCU clock under CONFIG_CLKSEL control.</td>
<td>If the CPU_CLK is not used to source the FCU clock, then pin should be tied to GND.</td>
</tr>
<tr>
<td>BYPASS_CLR_MEM</td>
<td>CFG</td>
<td>Input</td>
<td>Input to enable bypassing of the configuration memory clearing before device configuration.</td>
<td>Do not leave this pin unconnected. It should be tied to GND.</td>
</tr>
</table>

<table>
<tr><td>SCK</td><td>CFG</td><td>Output</td><td>Serial flash clock output. Clock can be sourced from either CPU_CLK (user driven) or on-chip oscillator (~10MHz). The on-chip ring-oscillator frequency may vary significantly over process and temperature. Please ensure that the Serial Flash Clock Divider setting is set to 2 or 4 to ensure that the maximum 6MHz configuration clock frequency requirement is not violated when the internal oscillator is used.</td><td>For SPI Mode: Connect directly to the flash device(s).
For CPU Mode: Leave unconnected.</td></tr>
<tr><td>SDI</td><td>CFG</td><td>Input / Output</td><td>In the SPI modes of operation, the serial data output pins for command and programming data to the flash memory. These command and programming commands are sent via control registers writes done via the IEEE 1149.1 JTAG interface. In the CPU mode, this pin is the bidirectional data bit 0, DQ[0].</td><td>Connect directly to the configuration controller. Do not leave this pin unconnected.</td></tr>
<tr><td>CSN[3:0]</td><td>CFG</td><td>Input / Output</td><td>In SPI Mode: The CSN[3:0] pins are active-low chip select outputs. In the programming mode, individual serial flash devices are mapped to a linear addressing space. In the SPI x1 configuration mode only the CSN[0] output is used.

In CPU Mode: CSN[3] is the bidirectional data bit 6, DQ[6]. CSN[2] is the bidirectional data bit 7, DQ[7]. CSN[1] is not used. CSN[0] is an active-low chip select input.</td><td>For SPI Mode: If SPIx1 is used, leave CSN[3:1] unconnected. In SPIx4, connect all four to the individual serial flash devices.

For CPU Mode: Connect CSN[3], CSN[2] and CSN[0] directly to the configuration controller. Tie CSN[1] to GND.</td></tr>
<tr><td>SD[3:0]</td><td>CFG</td><td>Input</td><td>Input pins providing data input from the flash device(s). In SPI x4 configuration mode, all 4 SD inputs are utilized. When in SPI x1 mode, only the SD[0] input is used to input the configuration data. In the CPU mode, these bits serve as the bidirectional data bits 1 through 4 (SD3=DQ1, SD2=DQ2, SD1=DQ3, SD0=DQ4)</td><td>Connect directly to the configuration controller. Do not leave these pins unconnected.</td></tr>
<tr><td>CONFIG_SYS_CLK_BYPASS</td><td>CFG</td><td>Input</td><td>Pin statically enabling the bypass of the internal SYS_CLK. The default clock for the FPGA configuration unit (FCU) is named SYS_CLK. An on-chip ring oscillator (~10MHz) is the source for SYS_CLK. For debug purposes this clock can be bypassed and an external clock supplied. The on-chip ring-oscillator frequency may vary significantly over process and temperature.
<table>
<tr><th>CONFIG_SYS_CLK_BYPASS</th><th>CONFIG_CLKSEL</th><th>CONFIG_MODESEL [2:0]</th><th>FCU CLK</th></tr>
<tr><td>0</td><td>0</td><td>001, 010</td><td>On-chip oscillator</td></tr>
<tr><td>1</td><td>0</td><td>001, 010</td><td>CPU_CLK</td></tr>
<tr><td>0/1</td><td>0</td><td>100</td><td>CPU_CLK</td></tr>
<tr><td>0</td><td>1</td><td>000, 001, 010, 100</td><td>TCK</td></tr>
</table>
</td><td>Do not leave this pin unconnected. It should be connected to a configurable input like a DIP switch to toggle between modes of operation for debug. If this is not possible or desired, tie this off to 1.8V (VDDO_JCFG / PA_VDD2) or GND based on the desired clock for the configuration mode.</td></tr>
</table>

START_CFG_STARTUP	CFG	Input	Used to restart the configuration startup state machine after the startup is already complete. This option is used if any errors are encountered in the configuration memory from ECC. NOT Available for HD1000.	For the HD1000 tie this pin to GND. For other devices, connect this pin directly to the configuration controller.
STAP_SEL	CFG	Input	When asserted high, this allows the JTAG interface pins to be directly connected to the JTAG controller in Serdes PMA blocks allowing SerDes configuration, debug and performance monitoring directly from the JTAG interface. For bitstream download and chip debug using the JTAG interface, this pin must be held low. For SerDes PMA debug only mode, this pin must be held high.	Do not leave this pin unconnected. It should be connected to a configurable input like a DIP switch to toggle between modes of operation for debug.
READ_STATE_ERR	CFG	Output	Debug output signal in fabric testing.	Leave unconnected.
CONFIG_SCRUB_MULTIPLE_ERR	CFG	Output	Indicates the presence of multiple errors when the SCRUB feature is used. NOT Available for HD1000.	For the HD1000, leave unconnected. For other devices, connect directly to observation point for error.
CONFIG_SCRUBBING_ENABLE	CFG	Input	Enables SCRUB feature for SEU mitigation in the configuration memory. NOT Available for HD1000.	For the HD1000 tie this pin to GND. For other devices, connect this pin directly to the configuration controller.
CONFIG_SCRUB_SINGLE_ERR	CFG	Output	Indicates the presence of a single error when the SCRUB feature is used. NOT Available for HD1000.	For the HD1000, leave unconnected. For other devices, connect directly to observation point for error.
General Purpose I/O Interface				
RCOMP_TERM_B [00,01,02,10,11,12,20,21,22, 30, 31,32,40,41,42,50,51,52]	BWN, BWC, BWS, BES, BEC, BEN	Input	Termination resistor input for dynamic drive compensation for PVT and aging. Used only when the PVT compensation controller is activated.	Terminate to GND through a swappable resistor. Currently a 200Ω +/- 1% resistor is being used internally. Resistor need not be used if I/O bank is unused.
RCOMP_DRV_B [00,01,02,10,11,12,20,21,22, 30, 31,32,40,41,42,50,51,52]	BWN, BWC, BWS, BES, BEC, BEN	Input	Drive resistor input for dynamic drive compensation for PVT and aging. Used only when the PVT compensation controller is activated.	Terminate to GND through a swappable resistor. Currently a 25Ω +/- 1% resistor is being used internally. Resistor need not be used if I/O bank is unused.
PAD_[WS/WC/WN/ES/EC/EN]_BYTEIO [12:0]DQ[9:0]	BWN, BWC, BWS, BES, BEC, BEN	Input / Output	A group of 13 byte lanes. Each byte lane has 12 bits; 10 of these 12 bits are used as data for memory interface applications. Alternatively, these I/Os could be set for Single Ended, Differential, LVCMOS, *STL and LVDS modes.	Unused I/Os can be left unconnected.
PAD_[WS/WC/WN/ES/EC/EN]_BYTEIO [12:0]DQS	BWN, BWC, BWS, BES, BEC, BEN	Input / Output	A group of 13 byte lanes. Each byte lane has 12 bits; the 11th bit carries a synchronous strobe signal (positive polarity differential clock) for referencing DQ[9:0] in each of the byte lanes. Alternatively, these I/Os could be set for Single Ended, Differential, LVCMOS, *STL and LVDS modes.	Unused I/Os can be left unconnected.
PAD_[WS/WC/WN/ES/EC/EN]_BYTEIO [12:0]DQSN	BWN, BWC, BWS, BES, BEC, BEN	Input / Output	A group of 13 byte lanes. Each byte lane has 12 bits; the 12th bit carries a synchronous strobe signal (negative polarity differential clock) for referencing DQ[9:0] in each of the byte lanes. Alternatively, these I/Os could be set for Single Ended, Differential, LVCMOS, *STL and LVDS modes.	Unused I/Os can be left unconnected.

Clock I/O Interface				
RCOMP_TERM_CLK_BANK_[NW/SW/SE/NE]	CB0, CB1, CB2, CB3	Input	Termination resistor input for dynamic drive compensation for PVT and aging. Used only when the PVT compensation controller is activated.	Terminate to GND through a swappable resistor. Currently a 200Ω +/- 1% resistor is being used internally. Resistor need not be used if clock bank is unused.
RCOMP_DRV_CLK_BANK_[NW/SW/SE/NE]	CB0, CB1, CB2, CB3	Input	Drive resistor input for dynamic drive compensation for PVT and aging. Used only when the PVT compensation controller is activated.	Terminate to GND through a swappable resistor. Currently a 25Ω +/- 1% resistor is being used internally. Resistor need not be used if clock bank is unused.
PAD[5:0]_CLK_BANK_[NW/SW/SE/NE]	CB0, CB1, CB2, CB3	Input / Output	A group of six clock buffers that can be used either as three differential I/Os or six single-ended I/Os. If these I/Os are not used as clock buffers, they can be used as generic inputs or outputs.	Unused I/Os can be left unconnected.
Miscellaneous				
CORE_TESTIN1	DBG	Output	Debug interface used for testing the fabric	Leave unconnected.
EDM	DBG	Output	For factory use / test purposes	Leave unconnected.
TEMP_DIODE_P/N	TEMP	Input	Die temperature monitoring diode connections (P and N).	If the temperature monitoring feature is not used, leave unconnected. Otherwise connect appropriately to the temperature sensor.
EFUSE_PROG	EFUSE	Output	HD1000's Efuse erase / program sequencer controls this signal. This signal should not be touched by user.	Leave unconnected.
Power				
PA_VDD1	N12P75G	Power	SerDes Analog Low Power Supply	0.95V analog power supply for the SerDes. Connect these pins to a linear or low noise switching power supply.
PA_VDD2	N12P75G	Power	SerDes Analog High Power Supply	Connect all 1.8V PA_VDD2 pins to a linear or low noise switching power supply. Highly sensitive SerDes analog power supply.
PA_VREG_CMN	N12P75G	Power	SerDes Regulator Power Supply	0.95V power supply for the SerDes regulator. Connect to PA_VDD1 through ferrite bead.
PA_VREG_RX	N12P75G	Power	SerDes Regulator Power Supply	0.95V power supply for the SerDes regulator. Connect to PA_VDD1 through ferrite bead.
PA_VREG_SYNTHX	N12P75G	Power	SerDes Regulator Power Supply	0.95V power supply for the SerDes regulator. Connect to PA_VDD1 through ferrite bead.
PAD_TE_I_A_RXTERMV_LNUM[31:0]	N12P75G	Power	Receiver Termination Voltage Pad input	Use a 1nF bypass cap and terminate to GND.
PA_VDD1	S12P75G	Power	SerDes Analog Low Power Supply	0.95V analog power supply for the SerDes. Connect these pins to a linear or low noise switching power supply.

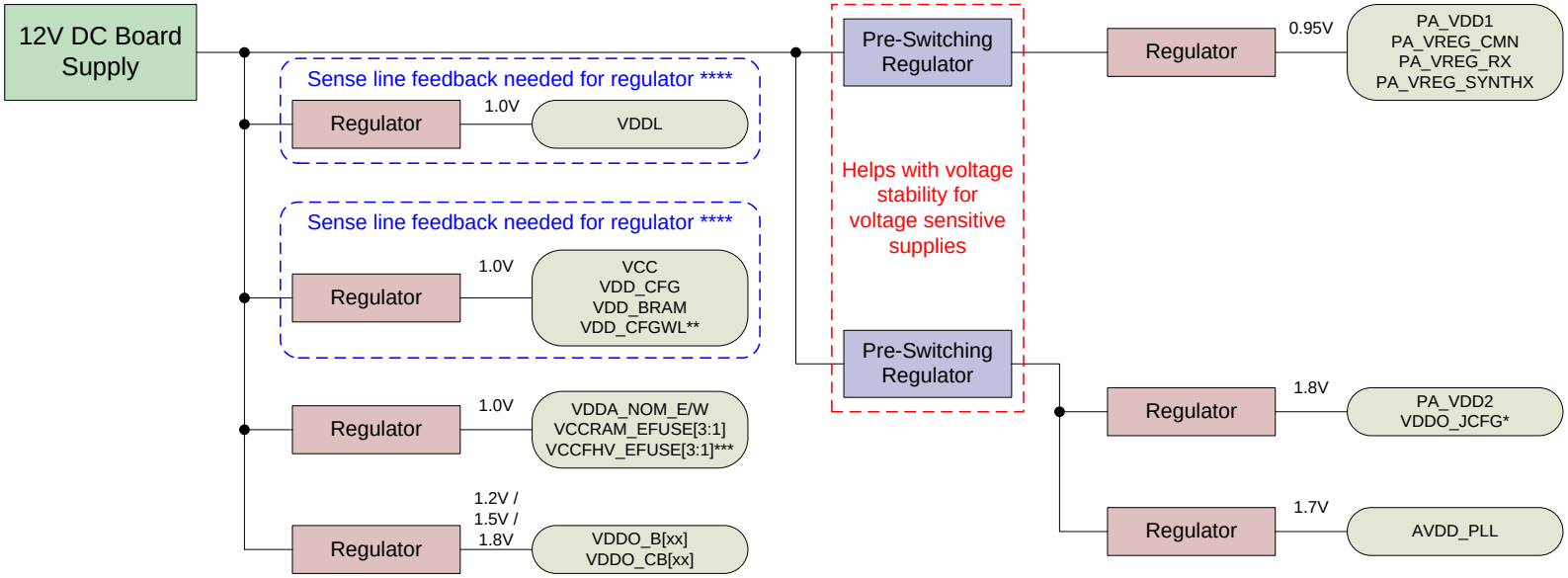
PA_VDD2	S12P75G	Power	SerDes Analog High Power Supply	Connect all 1.8V PA_VDD2 pins to a linear or low noise switching power supply. Highly sensitive SerDes analog power supply.
PA_VREG_CMN	S12P75G	Power	SerDes Regulator Power Supply	0.95V power supply for the SerDes regulator. Connect to PA_VDD1 through ferrite bead.
PA_VREG_RX	S12P75G	Power	SerDes Regulator Power Supply	0.95V power supply for the SerDes regulator. Connect to PA_VDD1 through ferrite bead.
PA_VREG_SYNTHX	S12P75G	Power	SerDes Regulator Power Supply	0.95V power supply for the SerDes regulator. Connect to PA_VDD1 through ferrite bead.
PAD_BE_I_A_RXTERMV_LNUM[31:0]	S12P75G	Power	Receiver Termination Voltage Pad input	Use a 1nF bypass cap and terminate to GND.
AVDD_PLL_[SE, SW, NE, NW][3:0]	PLL	Power	Analog power supply for the PLLs feeding the FPGA core fabric.	Connect all 1.7V AVDD_PLL pins to a linear or low noise switching power supply. This is a highly sensitive PLL analog power supply.
VDDO_JCFG	CFG	Power	Supply voltage powering the I/O buffers for the IEEE 1149.1 JTAG interface. The value selected determine the output VOH level on TDO and set the input threshold VIL and VIH values appropriately. (TAP) controller state machine transitions. This input is captured on the rising edge of the test logic clock (TCK). This dedicated pin is equipped with a pull-up resistor to place the test logic in the Test-Logic-Reset state	Connect these pins to a 1.8V power supply. This supply can be shared with the 1.8V analog SerDes power supply (PA_VDD2). Noise should not be a concern, since the JTAG I/O buffers and SerDes will generally not operate the same time. The one exception is during in-system debug with Snapshot, which should still be fine. However, it would be preferable to have this power supply be shared with a 1.8V VDDO_B[xx] I/O power supply if 1.8V I/Os are used in the design.
VDDL	CVDD	Power	Power Supply for FPGA fabric core logic	VDDL is the 1.0V core supply. Connect all VDDL pins to a low noise switching regulator. While VDDL is one of many 1.0V supplies, it is recommended that a separate regulator be used to ensure noise isolation and for prevention of current spikes prior to clearing of the configuration memory. Refer to the supply power up/down requirements below for further information.
VCC	SVDD	Power	Digital Power Supply for FPGA circuitry in the I/O ring, including the Hard IP.	Connect VCC to a 1.0V linear regulator. This supply can be shared with VDD_CFG and VDD_BRAM.
VCCRAM_EFUSE[3:1]	EFUSE	Power	Efuse Power Supply normal / read operations	Tie this to the 1.0V supply powering VDDA_NOM_E/W

VCCFHV_EFUSE[3:1]	FFUSE	Power	Efuse Power Supply for Fuse Program / Erase operations	If the application requires fuse blowing (eg. Encryption for design security), supply should be tied to a regulator providing output voltages in the 1.0V – 2.2V range. In such cases, this supply cannot be shared with any other supply. If fuse blowing is not needed, this supply can be tied to the 1.0V regulator powering VDDA_NOM_E/W and VCCRAM_EFUSE[3:1].
VDDA_NOM_E	EVDDA	Power	Analog Power Supply for FPGA circuitry in the I/O ring.	Connect VDDA_NOM_E to a 1.0V linear regulator. The only 1.0V supplies that can be shared with this supply are the eFuse power supplies.
VDD_CFG	CFG	Power	Supply voltage for the configuration memory SRAM cells in the FPGA fabric.	Connect VDD_CFG to a 1.0V linear regulator. This supply can be shared with VCC and VDD_BRAM.
VDD_CFGWL	CFG	Power	Power Supply for the wordlines of the configuration memory SRAM cells in the FPGA fabric.	For configuration memory readback capability (primarily for debug purposes), this supply would need to be set to 0.9V using a separate regulator. If this capability is not needed or desired, this supply can be more simply set to 1.0V and shared with VDD_CFG, VCC and VDD_BRAM.
VDDA_NOM_W	WVDDA	Power	Analog Power Supply for FPGA circuitry in the I/O ring.	Connect VDDA_NOM_W to a 1.0V linear regulator. The only 1.0V supplies that can be shared with this supply are the eFuse power supplies.
VDD_BRAM	VDD_BRAM	Power	Power Supply for Block RAMS in Fabric.	Connect VDD_BRAM to a 1.0V linear regulator. This supply can be shared with VCC and VDD_CFG.
VREF_B[00,01,02,10,11,12,20,21,22, 30, 31,32,40,41,42,50,51,52]	VDD_BANK	Power	Analog input; Voltage Bias reference. Half of corresponding bank / cluster voltage level.	Connect to a biasing circuit like a termination regulator with a reference based on the corresponding I/O cluster's power supply and terminate to ground using a 0.1uF bypass cap. If the bank uses IO standards not requiring references, or if the bank is unused, connect to ground.
VDDO_B[00,01,02,10,11,12,20,21,22, 30, 31,32,40,41,42,50,51,52]	VDD_BANK	Power	Bank I/O supply voltage. An I/O bank is defined as a group of byte-lanes that have a common power ball eg. 00. 3 I/O banks make up an I/O cluster eg. 00, 01, 02. X0 and x1 I/O banks have 4 byte lanes each and x2 I/O banks have 5 byte lanes to give a total of 13 byte-lanes or (13x12) 156 I/O pins. ***Note: Even though each I/O bank has a separate power ball, all 3 I/O banks in the I/O cluster are required to be set to the same voltage due to internal power rail sharing.***	The I/O supply voltage can be set to 1.2V, 1.5V or 1.8V. The I/O standard can be configured at a single I/O pin granularity, but because all I/Os in the same I/O cluster share a common supply, the standards need to be voltage compatible. Unused I/O banks should be powered. The power balls should NOT be left floating or grounded.

VREF_CLK_BANK_[SE, SW, NE, NW]	VDD_BANK	Power	Analog input; Voltage Bias reference for clock banks. Half of corresponding bank voltage level.	Connect to a biasing circuit like a termination regulator with a reference based on the corresponding clock bank's power supply and terminate to ground using a 0.1uF bypass cap. If the IO bank will use IO standards that do not require voltage references, the pins should be grounded.
VDDO_CB[SE, SW, NE, NW]	VDD_BANK	Power	Clock bank I/O supply voltage	The I/O supply voltage can be set to 1.2V, 1.5V or 1.8V. The I/O standard can be configured at clock bank corner granularity. Unused clock banks should be powered. The power balls should NOT be left floating or grounded.
VSS	VSS	Power	Ground	All GND pins should be connected to the board ground plane.

Power Supplies and Sequencing

Power Supply Block Diagram



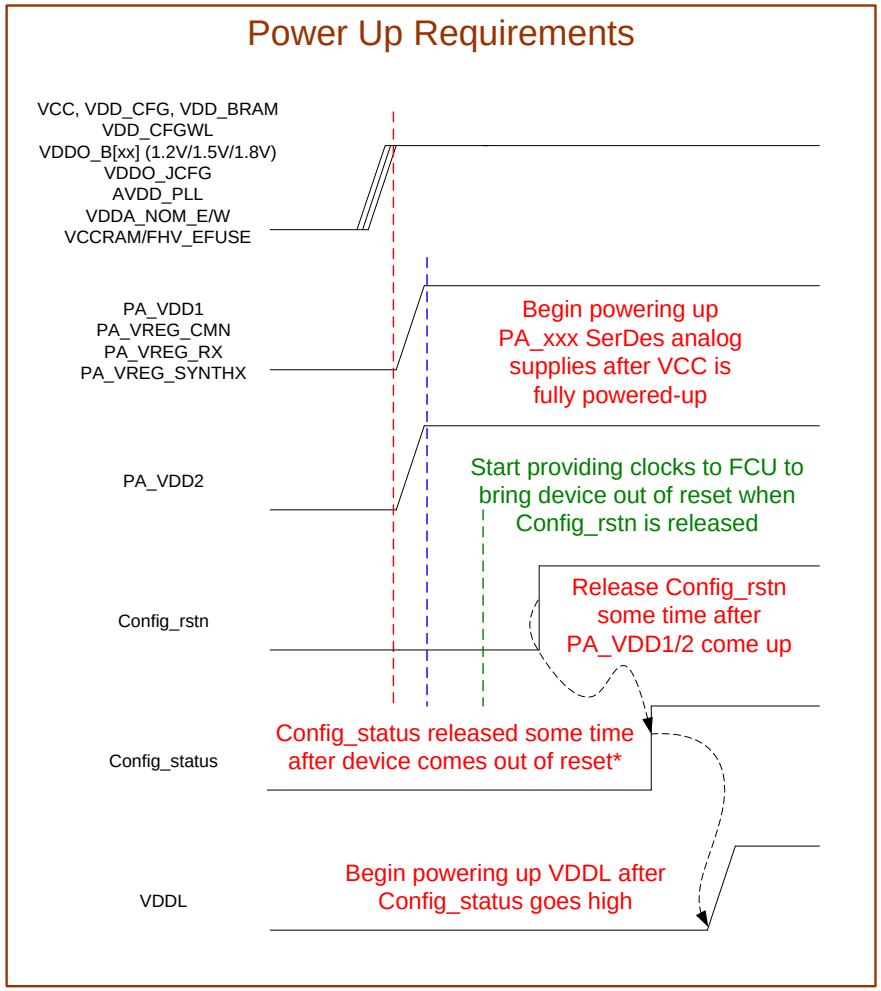
* It is preferable to share VDDO_JCFG with a voltage compatibale VDDO_B[xx] supply if a 1.8V IO Standard is being used in the design.

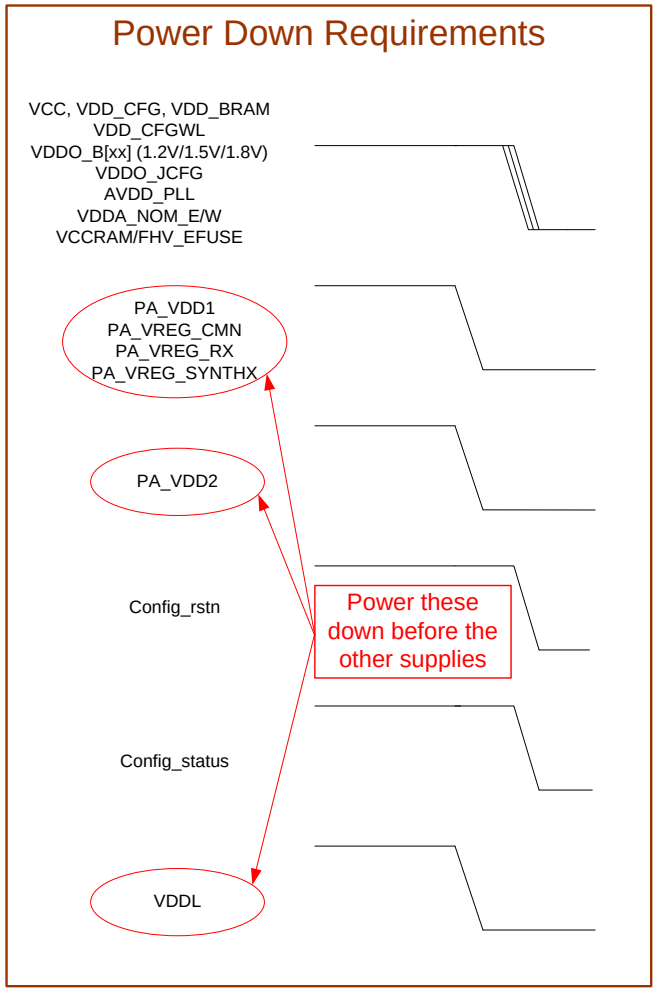
** For reliable configuration memory readback capability (primarily for debug), VDD_CFGWL needs to be set to 0.9V. Use a separate regulator to implement this. If readback capability is not desired, or if this implementation is not possible, VDD_CFGWL can be set to 1.0V.

*** For applications requiring the blowing of fuses (eg. encryption keys for design security), VCCFHV_EFUSE[3:1] must be powered by a separate regulator capable of providing voltages in the 1.0V – 2.2V range. Refer to the Design Security section of the Configuration User Guide UG033 for implementation details.

**** For these supplies with higher static and dynamic current needs, sense lines are needed to ensure that feedback is provided to the regulators to compensate for IR drops in the system. For the VCC / VDD_BRAM / VDD_CFG / VDD_CFGWL supply, voltage sensing on the VCC and VDD_BRAM supplies is most critical.

Power Sequencing Block Diagram





* When the device powers up, the CONFIG_STATUS output pin may temporarily be in an unknown state. The CONFIG_STATUS signal should not be monitored if a CONFIG_RSTN pulse has not been issued. After a pulse has been issued on CONFIG_RSTN, CONFIG_STATUS can be monitored. When CONFIG_STATUS goes high after that point, VDDL can be powered-up.

Revision History

The following table shows the revision history for this document.

Date	Version	Revisions
04/05/2013	1.0	Initial Achronix release.
04/12/2013	1.1	Reduced unique power supply requirements.
04/16/2013	1.2	Clarified connection requirements for some SerDes pins.
04/29/2013	1.3	Corrected connection scheme and pull up value (1.8V) for configuration pins
05/17/2013	1.4	Updated multiple entries in the pin connections to align with pin table.
06/11/2013	1.5	Additional information on some config I/Os and made User I/O section more concise.
07/26/2013	1.6	Clarifications for the CONFIG_STATUS and CONFIG_DONE I/Os.
10/17/2013	1.7	VDD_CFGWL update and CONFIG_RSTN assertion requirement during power-up.
11/07/2013	1.8	Modified JTAG/STAP_SEL, VDD_CFGWL and eFuse power supply requirements.
04/24/2014	1.9	Updated PCIe Gen3 requirements, sense lines and I/O power rail needs.
07/17/2014	1.10	Updated regulator needs for VDD_CFGWL and VREFs. Expanded explanations for other power supplies, and changed pull-up needs for some config pins.
08/19/2014	1.11	Updated SCK spec, JTAG TRSTN and corrected power supply block diagram.
07/12/2015	1.12	Updated FCU_CLK frequency and provided additional details on other pins. Clarified power-up diagram.
02/21/2016	1.13	Changed max FCU_CLK to be 6MHz. Added in notes for unused power and signal balls. Updated power-up sequencing figure to include all SerDes supplies.
03/07/2016	1.14	Updated description for BYPASS_CLR_MEM.