Speedster22i Capacitor User Guide

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Introduction

This document details the recommended types, sizes and placements of power supply capacitors for the Achronix HD1000 device. These recommendations have been crafted for the 52.5MM square package.

Recommendations

The following recommendations are based upon initial power integrity simulations of the HD1000 FBGA2597 package to an 18 layer 0.062" thick High Density Interconnect (HDI) style Printed Circuit Board (PCB). HDI PCBs typically feature laser micro vias, and the capability for both blind and buried vias. These capabilities can be used with large Ball Grid Array (BGA) devices to reduce the overall layer count, greatly improve signal integrity, and result in a more reliable PCB.

It is strongly recommended that customers perform their own power and signal integrity simulations based upon the chosen pin out, power supply design, PCB materials and stackup. The following recommendations assumed a worst case power supply current draw, as computed through the Achronix Power Estimator based on large numbers of I/Os at 1.5V or 1.35V switching rates, along with all SERDES operating at highest speed, and very large numbers of LUTs, flip-flops and BRAMs operating at high switching speed and high toggle rate. These conditions would never be true in a realistic FPGA design.

The following sections give per rail recommendations.

VDDO Capacitors

Using a DDR3 memory interface as a proxy for other kinds of high speed interfaces, three separate banks get combined together to make a DDR3 memory interface. In the case of the FBGA2597 HD1000 device, there are a total of six DDR3 memory interfaces. Accordingly, there would be a total of 6*3 = 18 banks representing all the standard I/O of the HD1000 device. The following table shows the DDR interface, and the banks associated with those DDR interfaces.

Table 1 - DDR Interfaces, banks, and VDDO pins

DDR Interface	Bank	Number of VDDO pins
West North (DDR_WN_xxx)	B00	5
	B01	5
	B02	5
West Center (DDR_WC_xxx)	B10	5
	B11	5
	B12	5
West South (DDR_WS_xxx)	B20	4
	B21	4
	B22	4
East North (DDR_EN_xxx)	B50	5
	B51	5
	B52	5
East Center (DDR_EC_xxx)	B40	5
	B41	5
	B42	5
East South (DDR_ES_xxx)	B30	5
	B31	5
	B32	5

Looking at the ball out of the FBGA2597 device, one will find the VDDO pins for any given bank to pretty much be in a row (or column) in such a way that they the VDDO pins may share a single 0201 ceramic capacitor. It should be possible to place a 1uF 20% X5R 4V ceramic capacitor. An example of this capacitor is a TDK C0603X5R0G105M030BC.

Table 2 - Example VDDO capacitor

VDDO Supply	Capacitor	Location	Value	Manu-facturer	Part Number
Decoupling	3x (18 total)	Each bank	1uF, 210%, X5R, 0201, 4V	TDK	C0603X5R0G105M030BC

VDDL Capacitors

The VDDL balls are balled -out in 9 rows. Place 5 0.1uF decoupling capacitors for each horizontal row, equal distant across each horizontal row. Place four 220uF bulk capacitors as near bulk. Place two of these within 500 mils on the south side of the package. Place the other two within 500 mils of the north side of the package. Additionally, each hemisphere of the FPGA within the 2-4 inches of the FPGA should receive: 1x 470uF, 5x 150uF capacitors, for a total of 12 bulk capacitors.

Table 3 - VDDL Capacitors

VDDL Supply	Capacitor	Location	Value	Manu-facturer	Part Number
Decoupling	5x (45 total)	Each horizontal row	0.1uF, 10%, X5R, 0201, 6.3V	Murata	GRM033R60J194KE19D
Near Bulk	2x	Within 500 mils of South Side	220uF, 10%, TANT, B, 2.5V	AVX	TPSB227K002R0150
Near Bulk	2x	Within 500 mils of North Side	220uF, 10%, TANT, B, 2.5V	AVX	TPSB227K002R0150
Bulk	1x	Place 2-4 in away from FPGA, Right hemisphere	470uF, 10%,,2917, 2.5V	AVX	TPSD477K002R0035
Bulk	5x	Place 2-4 in away from FPGA, Right hemisphere	150uF, 20%, X5R,1206, 4V	Taiyo Yuden	AMK316BBJ157ML-T
Bulk	1x	Place 2-4 in away from FPGA, Left hemisphere	470uF, 10%,,2917, 2.5V	AVX	TPSD477K002R0035
Bulk	5x	Place 2-4 in away from FPGA, Left hemisphere	150uF, 20%, X5R,1206, 4V	Taiyo Yuden	AMK316BBJ157ML-T

VCC Capacitors

The VCC balls are grouped in such a way that we can place four sets of decoupling capacitors to the north, south, east and west of the balls. For the north and south sides, place 3x 0.1uF capacitors. For the east and west sides, place 2x 0.1uF ceramic capacitors. Additionally, place the following bypass capacitors based on the ball out of the VCC balls: North side: 5x 1uF 0201s, South side: 5x 1uF 0201s, East side: 3x 1uF 0201s, West side 3x 1uF 0201s. Near bulk will consist of a set of 220uF caps within 500 mils of North and south side of package. Bulk capacitors are 1x 470uF and 2x 150uF within 2 to 4 inches of the FPGA package.

Table 4 - VCC Capacitors

VCC Supply	Capacitor	Location	Value	Manu-facturer	Part Number
Decoupling	3x	North side of VCC balls	0.1uF, 10%, X5R, 0201, 6.3V	Murata	GRM033R60J194KE19D
Decoupling	3x	South side of VCC balls	0.1uF, 10%, X5R, 0201, 6.3V	Murata	GRM033R60J194KE19D
Decoupling	2x	East side of VCC balls	0.1uF, 10%, X5R, 0201, 6.3V	Murata	GRM033R60J194KE19D
Decoupling	2x	West side of VCC balls	0.1uF, 10%, X5R, 0201, 6.3V	Murata	GRM033R60J194KE19D
Bypass	5x	North side of VCC balls	1uF, 20%, X5R, 0201, 4V	TDK	C0603X5R0G105M030BC
Bypass	5x	South side of VCC Balls	1uF, 20%, X5R, 0201, 4V	TDK	C0603X5R0G105M030BC
Bypass	3x	East side of VCC Balls	1uF, 20%, X5R, 0201, 4V	TDK	C0603X5R0G105M030BC
Bypass	3x	West side of VCC Balls	1uF, 20%, X5R, 0201, 4V	TDK	C0603X5R0G105M030BC
Near Bulk	2x	Within 500 mils of North Side	220uF, 10%, TANT, B, 2.5V	AVX	TPSB227K002R0150
Near Bulk	2x	Within 500 mils of South Side	220uF, 10%, TANT, B, 2.5V	AVX	TPSB227K002R0150
Bulk	1x	Place 2-4 in away from FPGA, Right hemisphere	470uF, 10%,,2917, 2.5V	AVX	TPSD477K002R0035
Bulk	2x	Place 2-4 in away from FPGA, Right hemisphere	150uF, 20%, X5R,1206, 4V	Taiyo Yuden	AMK316BBJ157ML-T
Bulk	1x	Place 2-4 in away from FPGA, Left hemisphere	470uF, 10%,,2917, 2.5V	AVX	TPSD477K002R0035
Bulk	2x	Place 2-4 in away from FPGA, Left hemisphere	150uF, 20%, X5R,1206, 4V	Taiyo Yuden	AMK316BBJ157ML-T

PA_VDD1 Capacitors

The PA_VDD1 decoupling capacitors will consists of 5x 0.1uF capacitors each of the four horizontal rows. Spread these out to be equal distance from any ball, roughly two balls per capacitor. Bypass will consist of 7x 1uF bypass capacitors each of the four horizontal rows. Spread these out to be equal distance from any ball, roughly two balls per capacitor. For near bulk, place 2x 220uF capacitors within 500 mils of west side and 2x 220uF capacitors within 500 mils of east side of package. For bulk capacitors, place 1x 470uF and 2x 150uF capacitors within 2 to 4 inches of south or east side of package and a duplicate of that on north or west side of package.

Table 5 - PA_VDD1 Capacitors

PA_VDD1 Supply	Capacitor	Location	Value	Manu-facturer	Part Number
Decoupling	20x	5x per row of balls (4 rows)	0.1uF, 10%, X5R, 0201, 6.3V	Murata	GRM033R60J194KE19D
Bypass	28x	7x per row of balls (4 rows)	1uF, 20%, X5R, 0201, 4V	TDK	C0603X5R0G105M030BC
Near Bulk	2x	Within 500 mils of North or West Side	220uF, 10%, TANT, B, 2.5V	AVX	TPSB227K002R0150
Near Bulk	2x	Within 500 mils of South or east Side	220uF, 10%, TANT, B, 2.5V	AVX	TPSB227K002R0150
Bulk	1x	Place 2-4 in away from FPGA, Right hemisphere	470uF, 10%,,2917, 2.5V	AVX	TPSD477K002R0035
Bulk	2x	Place 2-4 in away from FPGA, Right hemisphere	150uF, 20%, X5R,1206, 4V	Taiyo Yuden	AMK316BBJ157ML-T
Bulk	1x	Place 2-4 in away from FPGA, Left hemisphere	470uF, 10%,,2917, 2.5V	AVX	TPSD477K002R0035
Bulk	2x	Place 2-4 in away from FPGA, Left hemisphere	150uF, 20%, X5R,1206, 4V	Taiyo Yuden	AMK316BBJ157ML-T

PA_VDD2 Capacitors

The PA_VDD2 decoupling capacitors will consists of 5x 0.1uF capacitors each of the four horizontal rows. Spread these out to be equal distance from any ball, roughly two balls per capacitor. Bypass will consist of 7x 1uF bypass capacitors each of the four horizontal rows. Spread these out to be equal distance from any ball, roughly two balls per capacitor. For near bulk, place 2x 220uF capacitors within 500 mils of west side and 2x 220uF capacitors within 500 mils of east side of package. For bulk capacitors, place 1x 470uF and 2x 150uF capacitors within 2 to 4 inches of south or east side of package and a duplicate of that on north or west side of package.

Table 6 - PA_VDD2 Capacitors

PA_VDD2 Supply	Capacitor	Location	Value	Manu-facturer	Part Number
Decoupling	20x	5x per row of balls (4 rows)	0.1uF, 10%, X5R, 0201, 6.3V	Murata	GRM033R60J194KE19D
Bypass	28x	7x per row of balls (4 rows)	1uF, 20%, X5R, 0201, 4V	TDK	C0603X5R0G105M030BC
Near Bulk	2x	Within 500 mils of North or West Side	220uF, 10%, TANT, B, 2.5V	AVX	TPSB227K002R0150
Near Bulk	2x	Within 500 mils of South or east Side	220uF, 10%, TANT, B, 2.5V	AVX	TPSB227K002R0150
Bulk	1x	Place 2-4 in away from FPGA, Right hemisphere	470uF, 10%,,2917, 2.5V	AVX	TPSD477K002R0035
Bulk	2x	Place 2-4 in away from FPGA, Right hemisphere	150uF, 20%, X5R,1206, 4V	Taiyo Yuden	AMK316BBJ157ML-T
Bulk	1x	Place 2-4 in away from FPGA, Left hemisphere	470uF, 10%,,2917, 2.5V	AVX	TPSD477K002R0035
Bulk	2x	Place 2-4 in away from FPGA, Left hemisphere	150uF, 20%, X5R,1206, 4V	Taiyo Yuden	AMK316BBJ157ML-T

VCC_BRAM Capacitors

The VCC_BRAM decoupling capacitors will consists of 3x 0.1uF capacitors each of the four vertical columns. Spread these out to be equal distance from any ball, roughly two balls per capacitor. Bypass will consist of 20x 1uF bypass capacitors, one ball per capacitor. For near bulk, place 2x 220uF capacitors within 500 mils of package, nearest the VCC_BRAM balls.

Table 7 - VCC_BRAM Capacitors

VCC_BRAM Supply	Capacitor	Location	Value	Manu-facturer	Part Number
Decoupling	12x	3x per column of balls (4 col)	0.1uF, 10%, X5R, 0201, 6.3V	Murata	GRM033R60J194KE19D
Bypass	20x	One per ball	1uF, 20%, X5R, 0201, 4V	TDK	C0603X5R0G105M030BC
Near Bulk	2x	Within 500 mils of package, nearest VCC_BRAM rail	220uF, 10%, TANT, B, 2.5V	AVX	TPSB227K002R0150

VCC_NOMxx Capacitors

The VDDA_NOM capacitors will mix decoupling and bypass. Place four pairs of 0.1uF and 1UF 0201 capacitors interstitially amongst the VDDA_NOM_xx balls.

Table 8 - VCC_NOMxx Capacitors

VDDA_NOM Supply	Capacitor	Location	Value	Manu-facturer	Part Number
Decoupling	4x	Interstitial amongst VDDA_NOM balls	0.1uF, 10%, X5R, 0201, 6.3V	Murata	GRM033R60J194KE19D
Bypass	4x	Interstitial amongst VDDA_NOM balls	1uF, 20%, X5R, 0201, 4V	TDK	C0603X5R0G105M030BC

AVDD_PLLxx Capacitors

The AVDD_PLL_xx capacitors will mix decoupling and bypass. Place four pairs of 0.1uF and 1UF 0201 capacitors interstitially amongst the AVDD_PLL_xx balls.

Table 9 - AVDD_PLLxx Capacitors

AVDD_PLL_xx Supply	Capacitor	Location	Value	Manu-facturer	Part Number
Decoupling	4x	Interstitial amongst AVDD_PLL_xx balls	0.1uF, 10%, X5R, 0201, 6.3V	Murata	GRM033R60J194KE19D
Bypass	4x	Interstitial amongst AVDD_PLL_xx balls	1uF, 20%, X5R, 0201, 4V	TDK	C0603X5R0G105M030BC

PA_VREG_CMN Capacitors

The PA_VREG_CMN capacitors will mix decoupling and bypass. Place two pairs of 0.1uF and 1UF 0201 capacitors interstitially amongst the PA_VREG_CMN balls.

Table 10 - PA_VREG_CMN Capacitors

PA_VREG_CMN Supply	Capacitor	Location	Value	Manu-facturer	Part Number
Decoupling	2x	Interstitial amongst PA_VREG_CMN balls	0.1uF, 10%, X5R, 0201, 6.3V	Murata	GRM033R60J194KE19D
Bypass	2x	Interstitial amongst PA_VREG_CMN balls	1uF, 20%, X5R, 0201, 4V	TDK	C0603X5R0G105M030BC

PA_VREG_RX Capacitors

The PA_VREG_RX capacitors will mix decoupling and bypass. Place two pairs of 0.1uF and 1UF 0201 capacitors interstitially amongst the PA_VREG_RX balls.

Table 11 - PA_VREG_RX Capacitors

PA_VREG_RX Supply	Capacitor	Location	Value	Manu-facturer	Part Number
Decoupling	2x	Interstitial amongst PA_VREG_RX Balls	0.1uF, 10%, X5R, 0201, 6.3V	Murata	GRM033R60J194KE19D
Bypass	2x	Interstitial amongst PA_VREG_RX balls	1uF, 20%, X5R, 0201, 4V	TDK	C0603X5R0G105M030BC

PA_VREG_SYNTHX Capacitors

The PA_VREG_SYNTHX capacitors will mix decoupling and bypass. Place two pairs of 0.1uF and 1UF 0201 capacitors interstitially amongst the PA_VREG_SYNTHX balls.

Table 12 - PA_VREG_SYNTHX Capacitors

PA_VREG_SYNTHX Supply	Capacitor	Location	Value	Manu-facturer	Part Number
Decoupling	2x	Interstitial amongst PA_VREG_SYNTHX Balls	0.1uF, 10%, X5R, 0201, 6.3V	Murata	GRM033R60J194KE19D
Bypass	2x	Interstitial amongst PA_VREG_SYNTHX balls	1uF, 20%, X5R, 0201, 4V	TDK	C0603X5R0G105M030BC

PA_VREG_CFG Capacitors

The VDD_CFG capacitors will mix decoupling and bypass. Place two pairs of 0.1uF and 1UF 0201 capacitors interstitially amongst the VDD_CFG balls.

Table 13 - PA_VREG_CFG Capacitors

VDD_CFG Supply	Capacitor	Location	Value	Manu-facturer	Part Number
Decoupling	2x	Interstitial amongst VDD_CFG Balls	0.1uF, 10%, X5R, 0201, 6.3V	Murata	GRM033R60J194KE19D
Bypass	2x	Interstitial amongst VDD_CFG balls	1uF, 20%, X5R, 0201, 4V	TDK	C0603X5R0G105M030BC

PA_VREG_CFGWL Capacitors

The VDD_CFGWL capacitors will mix decoupling and bypass. Place two pairs of 0.1uF and 1UF 0201 capacitors interstitially amongst the VDD_CFGWL balls.

Table 14 - PA_VREG_CFGWL Capacitors

VDD_CFGWL Supply	Capacitor	Location	Value	Manu-facturer	Part Number
Decoupling	2x	Interstitial amongst VDD_CFGWL Balls	0.1uF, 10%, X5R, 0201, 6.3V	Murata	GRM033R60J194KE19D
Bypass	2x	Interstitial amongst VDD_CFGWL balls	1uF, 20%, X5R, 0201, 4V	TDK	C0603X5R0G105M030BC

VCCRAM_EFUSE Capacitors

The VCCRAM_EFUSE capacitors will mix decoupling and bypass. Place a pair of 0.1uF and 1UF 0201 capacitors interstitially amongst the VCCRAM_EFUSE balls.

Table 15 - VCCRAM_EFUSE Capacitors

VCCRAM_EFUSE Supply	Capacitor	Location	Value	Manu-facturer	Part Number
Decoupling	1x	Interstitial amongst VCCRAM_EFUSE Balls	0.1uF, 10%, X5R, 0201, 6.3V	Murata	GRM033R60J194KE19D
Bypass	1x	Interstitial amongst VCCRAM_EFUSE balls	1uF, 20%, X5R, 0201, 4V	TDK	C0603X5R0G105M030BC

Revision History

The following table shows the revision history for this document.

Date	Version	Revisions
4/10/2015	1.0	Initial Achronix release.