Speedcore eFPGA Test Chip Evaluation Board

EVALUATION BOARD HIGHLIGHTS

- Speedcore™ 16-nm FinFET+ Embedded FPGA IP test chip AC16tC01AC01A (see below for FPGA details)
- 32 programmable input and 32 programmable output GPIOs for test and user application design
- 24 of 32 programmable GPIO inputs combined to support 12-bit LVDS differential inputs
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- 8 inputs and 8 outputs of each of the remaining 32 programmable input/outputs used as GPIO
- Programmable clock sources and clock synthesizers supporting 500MHz, 100MHz, 16MHz and 10MHz
- Simple USB interface that supports JTAG, CPU and SPI configuration modes
- An additional dedicated USB DCC (Direct Cable Connection) interface for direct serial communication with the eFPGA’s Control and Status (CSR) register
- SPI EEPROM for FPGA configuration
- SMA connectors for driving external clocks and GPIO
- A 120 contact Samtec QSH-060-01-F-D-A connector for interfacing with an external A/D adapter card
- A 160 contact Samtec ASP-122953-01 connector for interfacing with an external D/A adapter card

Speedcore eFPGA Evaluation Board Supporting 16nm FinFET+ Speedcore Test Chip

The Speedcore eFPGA evaluation board from Achronix contains the Speedcore eFPGA test chip, a 16-nm programmable logic IP manufactured on TSMC’s 16nm FinFET+ process technology. The evaluation board’s Speedcore test chip has been customized with the right blend of resources such as LUTs, BRAMs, DSP64s, DFFs and a number of I/O so as to provide an optimum programmable platform for demonstrating, evaluating and testing Achronix’s Speedcore technology. This mix of resources, organization, power profile and die size were engineered using Achronix’s Speedcore Die Size Calculator which allow users to plan and build their own customized and scalable Speedcore eFPGA fabric solution geared towards their application specific device needs.

Clocks

The evaluation board has an 8T49N287 IDT FemtoClock NG Octal Universal Frequency Translator which is configured to generate various LVDS output clocks. The programmed output clocks available on the board are:

- 100 MHz LVDS reference clock for Speedcore eFPGA configuration
- 500 MHz LVDS for user application design
- 16 MHz LVDS for DCC
- 10 MHz for miscellaneous use
**Interfaces**

The list of Evaluation board connectors available on the board in reference to the block diagram above are as follows:

**Input Connectors**

- The SMA LVDS inputs are twelve pairs of SMA input connectors
- The NI input is a VHDCI 0.8mm 68-pin Vertical Receptacle Connector
- The A/D input is a Samtec QSH-060-01-F-D-A connector for connecting to the TI ADS5463EVM 12-bit A/D adapter card
- The TEST POST input is a standard 2 × 25 connector with 0.040" posts with 0.100" spacing
- The DCC input is a single CMOS input from the FT232R FTDI USB to the serial input circuit
- The GPIO TEST POST input is a 16-pin 2x8 connector with 0.040" posts with 0.100" spacing
- The GPIO SMA inputs are eight single-ended SMA connectors
- The Switches input is an 8-input DIP switch with pull-up resistors to 1.8V

**Output Connectors**

- The SMA LVDS outputs are twelve pairs of SMA input connectors
- The NI output is a VHDCI 0.8mm 68-pin Vertical Receptacle Connector
- The D/A output is a Samtec ASP-122953-01 HSDIO connector for connecting to the TI DAC3162EVM 12-bit D/A adapter card
- The TEST POST output is a standard 2x25 connector with 0.040" posts with 0.100" spacing
- The DCC output is a single CMOS input from the FT232R FTDI USB to serial input circuit
- The GPIO TEST POST output is a 16-pin 2x8 connector with 0.040" posts with 0.100" spacing
- The GPIO SMA outputs are eight single-ended SMA connectors
- The GPIO LED output are connected to eight surface-mount LEDs

**Power Supplies**

The following are the power supplies available on the Speedcore evaluation board:
• VCC 1.0V 20A (tied to VCFG and VDDL inside package/die) provided by LTM4677 Dual 18A µmodule step-down DC/DC Regulator
• VDDO 1.8V 5A (for 1.8V LVCMOS and LVDS) provided by LMT4633 triple 10A step-down DC/DC µmodule regulator
• VREF 1.2V 4A provided by LMT4633 triple 10A step-down DC/DC µmodule regulator
• 2.5V 5A supply for the clock multiplexers/de-multiplexers provided by LMT4633 triple 10A step-down DC/DC µmodule regulator
• 3.3V 3A for the USB FTDI programming interface provided by an external PC power supply
• 5V 1A for the USB DCC interface provided by an external PC power supply
• 12V 5A external PC board power supply which supplies the necessary DC-DC power to drive the various components on the evaluation board

Speedcore eFPGA Test Chip (AC16tTC01AC01A) Features
• Speedcore Embedded FPGA IP – The only company shipping eFPGA technology in production applications.
• Process: TSMC 16nm FiFET+ (16FF+)
• Custom Speedcore eFPGA test chip resource counts for logic, embedded memory blocks and DSP blocks:
  • 40K LUTs – 4-input look-up-tables (LUTs) plus integrated wide MUX functions and fast adders
  • 48 Block RAMs (BRAM) – 20 kb per memory block (optional)
  • Logic RAM (LRAM) – 4 kb per memory block (optional)
  • 72 DSP64 – each block has a 18 × 27 multiplier, 64-bit accumulator and 27-bit pre-adder
  • 64 programmable user I/Os for fabric evaluation
• Speedcore performance: 750 MHz (max), 300–400 MHz (typical).
• Achronix delivers the eFPGA IP as a hard macro in GDSII format.
• Lowest latency interface:
  • One stage of latency between a Speedcore instance and the host SoC
  • Support for zero-latency interfaces
• Lowest FPGA power: 0.7 µW static power per 1,000 LUTs (on the TSMC 16FF+ process)

Design Methodology
The Achronix CAD Environment (ACE) software development tools act as the software-stack to enable successful integration and functionality of the Speedcore eFPGA. ACE is a full-featured FPGA design environment that delivers best-in-class quality of results for performance, area and compile times.

The ACE design tool suite includes Synplify Pro from Synopsys for RTL synthesis. ACE takes the synthesized design netlist and provides placement, routing, timing analysis, bitstream generation and FPGA configuration. For verification, ACE supports multiple industry standard simulators and includes Snapshot logic analyzer for real-time, on-chip design debugging. The Speedcore eFPGA Evaluation Board kit includes a one-year license for both ACE and Synplify Pro for Achronix.

Device Configuration
The Speedcore eFPGA and other components on the test chip Evaluation board are fully controlled from within the ACE design software. Users simply plug a USB cable from their computer into the board to do the following:
• Configure the Speedcore eFPGA using JTAG, Flash or CPU mode
• Use the I²C interface to program the power regulators and clock synthesizers plus read the temperature sensors, voltages and currents
• Use Achronix’s Snapshot real-time design debug tool to monitor signals in the Speedcore eFPGA

Application Demo Design

The Speedcore evaluation board comes pre-loaded with an example application design shown above, which is a notch filter operating at 245 MHz that results in the Speedcore eFPGA fabric running at at least $2 \times 245 \text{ MHz} = 490 \text{ MHz}$ sampling rate as per the Nyquist (2× sampling) theorem.

Summary

The Speedcore eFPGA Test Chip Evaluation board is an ideal platform for the Achronix Speedcore eFPGA IP evaluation. Through the ACE software tool suite, the user is given the ability to generate new designs or utilize pre-existing demo ones to program the Speedcore eFPGA to do an evaluation of its capabilities and performance. The circuitry on the board provides for stimulus and observation capabilities allowing users to take advantage of options and flexibility, as well as viewing real-time results from their tests.