Speedchip FPGA Chiplets

Speedchip Highlights

- Speedchip™ FPGA chiplet, optimized for multi-chip packaging solutions
- Customer-defined FPGA resource counts for logic, embedded memory blocks, DSP blocks, and I/O interfaces
  - Logic – high-performance look-up-tables (LUTs) plus integrated wide MUX functions and fast adders. Logic densities can range from 50k to 1M LUTs.
  - Logic RAM – 4 kb per memory block
  - Block RAM – 20 kb per memory block
  - DSP64 – each block has a 18 × 27 multiplier, 64-bit accumulator and 27-bit pre-adder plus pipeline register stages
- Customer-defined integration options
  - 2.5D package integration on a silicon or organic interposer
  - Multi-chip module (MCM)
- Speedchip FPGA chiplet typical core performance: 300 to 500 MHz
- Die-to-die communication between Speedchip FPGA chiplet and ASIC via industry-standard, third-party, high-speed interconnect technology using USR SerDes. Contact Achronix for more details

Benefits

- Significantly lower cost and power than equivalent density standalone FPGAs – optimally sized for the end application, eliminates high-power programmable I/O
- Mix and match ASIC and Speedchip FPGA chiplets to create multiple product SKUs
- Reuse chiplets across different platforms and applications
- Delivers similar integration as eFPGAs, while decoupling the process technology of the FPGA from the ASIC

Design and Development

- Speedchip FPGA chiplets are supported by Achronix ACE design tools:
  - Full-featured tools to synthesize, place, route and optimize RTL performance for a Speedchip-based design
  - Includes Synplify Pro for synthesis

Next-generation SoC platforms are evolving rapidly to process and move enormous amounts of data from the edge; over the network and to the cloud for high data and compute intensive applications such as AI and machine learning, high-performance computing (HPC) and autonomous driving. As a result, next-generation ASICs need to be larger, faster and further optimized for performance, power and area compared to their predecessors. Most importantly, these same platforms need to be flexible to allow for changing standards, evolving algorithms, and reconfigurable processing structures.

Among the spectrum of programmable solutions that include CPUs and GPUs, FPGAs offer the highest compute capacity with the lowest power profile. However, discrete FPGAs functioning as hardware accelerators alongside processors and other compute solutions are expensive and require significant board space for the FPGA plus supporting components. Speedchip FPGA chiplets are a better solution that brings FPGA functionality closer to other system chips, which enables higher bandwidth, reduced system latency, and reduced system cost. Integrating an FPGA chiplet and ASIC die in the same package is an ideal solution for companies looking to bring the programmability and flexibility of an FPGA to their next-generation high-performance system-in-package (SiP) solutions.

Speedchip FPGA Chiplets

Speedchip FPGA chiplets are optimized for embedding in advanced system-in-package (SiP) solutions such as 2.5D via silicon interposer or organic substrate. With Speedchip chiplets, customers define the functionality for their FPGA chiplet by specifying the number of LUTs, memory blocks, DSP blocks and I/O interfaces needed for their application. Achronix then develops the Speedchip chiplet tailored to the customer's specification, delivering the first samples within 6 to 8 months for integration in a SiP solution.
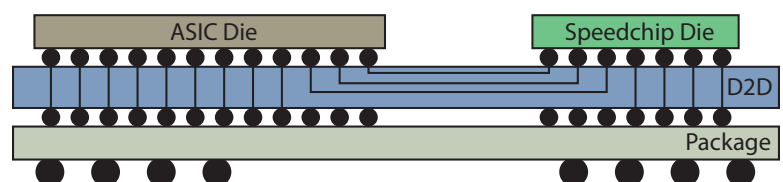
The integrated Speedchip FPGA chiplet communicates with the host ASIC via industry-standard, high-speed interconnect technology such as USR SerDes.

Customers work with their preferred packaging system vendor to integrate the Speedchip FPGA chiplet into their SiP. For examples, designers can partition the SiP sub-system using either die-to-interposer stacking or die-to-wafer stacking, where finished die are bonded on top of a fully processed wafer. Die are then interconnected using through-Si vias (TSVs) and micro-bumps.

Benefits

Integrating a Speedchip chiplet in a SiP has significant advantages over a traditional monolithic die, where the latter has several components such as the processor, high-bandwidth memories, and other digital logic, placed on a single large monolithic die.

- Low-latency, low-power since the length of the wires between the ASIC and FPGA chiplet is significantly shorter than chip-to-chip connections.

- Higher levels of integration with processor and memory cores due to a smaller footprint of the FPGA chiplet.

- Ability to combine components at different process technologies on the same package. For example, the high functionality Speedchip FPGA chiplet can be built on an advanced process node such as 7nm while other digital logic could be on a older technology node such as 28nm or 40nm.

- Using multiple chiplets results in a lower cost solution versus a large die-size monolithic SoC.

- Improved electrical and reliability performance of the system.

Configuring Speedchip Chiplets

Speedchip FPGA chiplets can be configured via three different interfaces — JTAG, Flash and CPU. Each Speedchip instance contains its own FPGA configuration unit (FCU) that initializes, configures, and manages the Speedchip core logic array. Each FCU has a set of configuration and mode pins used to determine how the configuration pins will operate.
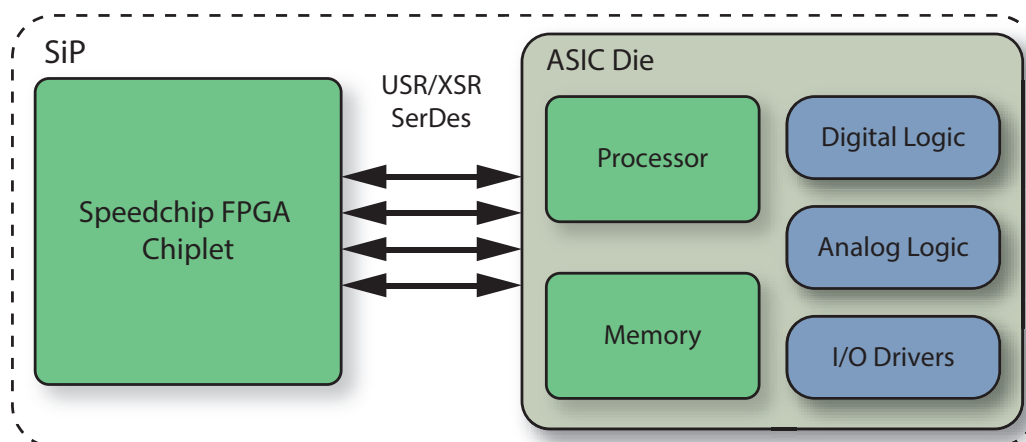
Speedchip FPGA Chiplets Supports a Range of Applications

High-performance computing, networking and storage applications require enormous interconnect bandwidth between co-packaged dice. Speedchip FPGA chiplets can be used for application-specific workload acceleration applications in networking and communications infrastructure such as encryption, decryption and compression, packet processing, traffic management and 5G physical layer signal processing. In addition, customers can use Speedchip chiplets for high-performance compute acceleration workloads such as data centers, high-frequency trading and autonomous driving.

About Achronix

Achronix Semiconductor Corporation is a privately held, fabless semiconductor corporation based in Santa Clara, California and offers high-performance FPGA solutions. Achronix's history is one of pushing the boundaries in the high-performance FPGA market.

Achronix offerings include programmable FPGA fabrics, FPGA Chiplets, discrete high-performance and high-density FPGAs with hardwired system-level blocks, datacenter and HPC hardware accelerator boards, and best-in-class EDA software supporting all Achronix products.

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