

PCIe Enumeration of Speedster7t FPGAs (AN027)



March 02, 2023

Application Note

Introduction

PCIe device enumeration is necessary to allow a device with a PCIe interface to be discovered in a system. This application note provides the steps to attain enumeration from a non-enumerated device with a PCIe interface and from an already enumerated device. Use these steps to enumerate a Speedster®7t FPGA configured as a PCIe endpoint device.

Using the Achronix Device Manager for PCIe



Warning!

Designs that use a PCIe interface should include the Achronix Device Manager in order to facilitate proper enumeration.

The PCIe controller works in conjunction with the Achronix Device Manager. Refer to the following steps to use the Achronix Device Manager with the PCIe Interface.



Note

The use of the Device Manager for PCIe is supported for ACE 9.0 and onward. For ES0 devices (partname = AC7t1500ES0 in ACE) the Achronix Device Manager does not need to be included in the design.

1. Add either the Speedster7t GPIO Bank IP file or the Speedster7t Clock I/O Bank IP file to the ACE project. Use a GPIO or REFIO ball to bring the PCIe PERST signal into the FPGA fabric.

Note
For the VectorPath® S7t-VG6 accelerator card, use ball N16 for the x16 PCIe interface.

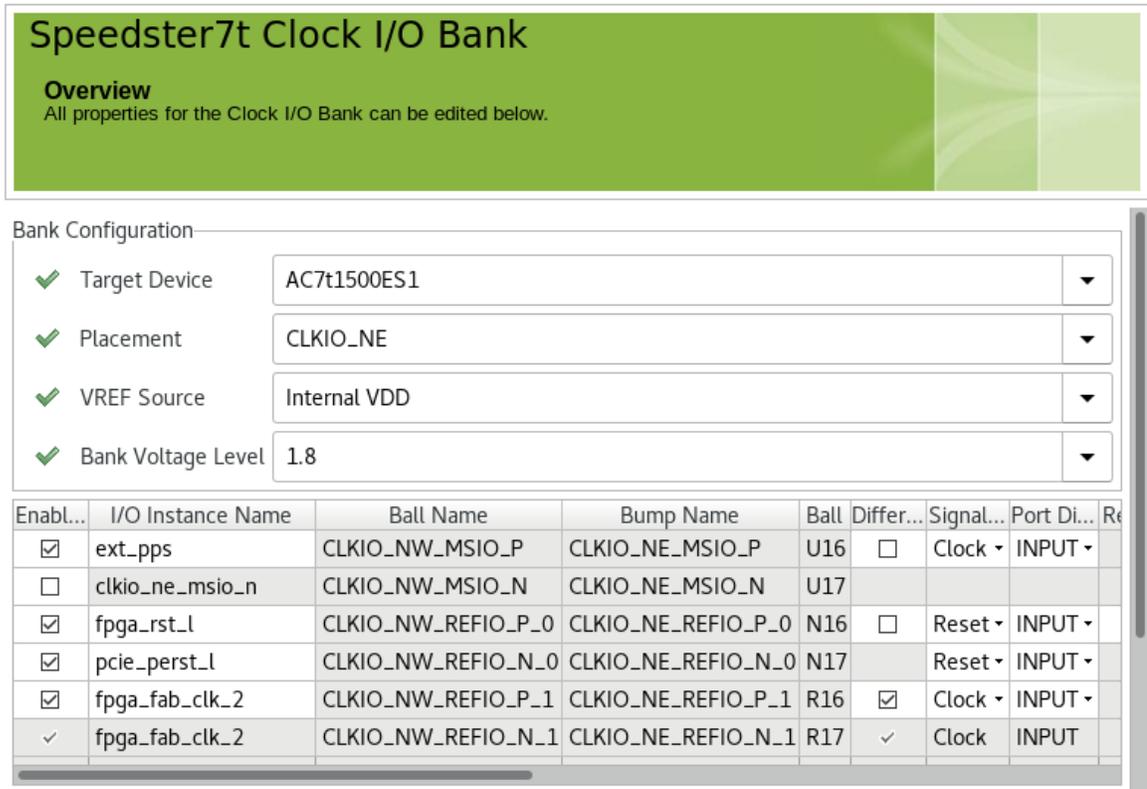


Figure 1: Speedster7t Clock I/O Bank IP File in ACE GUI

2. Add the Speedster7t Device Manager IP and expose the PERSTN input for the PCIe interface being used.

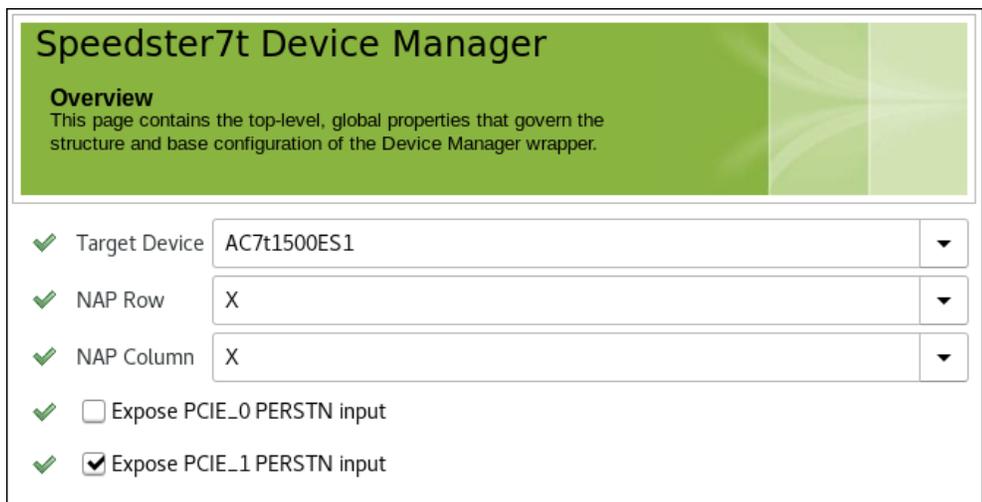


Figure 2: Speedster7t Device Manager IP file in ACE GUI

3. Generate I/O ring files and the Achronix Device Manager SystemVerilog wrapper file.
4. Instantiate the Device Manager in the RTL and connect the PERST signal to the appropriate `i_pcie_0_perstn/i_pcie_1_perstn` input port.

Achronix Device Manager Wrapper Instance Example

```

acx_device_manager x_acx_dev_mgr (
    // JTAG ports
    .i_jtag_in      (i_jtag_in),          // Should be connected to top-level ports with the
    same declaration
    .i_tdo_bus      (tdo_bus),           // Pass-through the JTAG bus to connect to
    Snapshot. If not used, this input should be tied to 1'b0
    .o_jtag_out      (o_jtag_out),       // Should be connected to top-level ports with
    the same declaration
    .o_jtap_bus     (jtap_bus),          // output t_JTAP_BUS - Pass-through of the
    JTAG bus to connect to Snapshot (or other JTAG components)

    .i_pcie_1_perstn(fpga_rst_1),        // PERST pin for PCIE1 <<<---- ADD THIS PORT

    // User Design
    .i_clk          (i_dev_mgr_clk),     // 100 MHz Clock input for Device Manager block
    .i_start        (dev_mgr_pll_lock),  // A high input starts the Device Manager. In
    most cases this signal is simply tied to 1'b1, but it can also be tied to a PLL lock signal
    if necessary.
    .o_status       (o_status)           // Progress indication, error status, alarms
);

```

Device Enumeration

Initial PCIe Device Enumeration

If the device is powered on and has not enumerated, follow these steps to discover the device:

1. Program the FPGA with the desired bitstream. For more information on programming the FPGA, refer to the [Speedster7t Configuration User Guide \(UG094\)](#).
2. Enter the following command to perform a warm reboot on the system.

```
$ sudo -S systemctl --force --force reboot
```

3. Ensure that the device has been enumerated by using the `lspci` command as shown to display PCI devices and identify the device. The `-d` flag can be used to show only devices with the specified vendor, device, and class ID. The numbers are given in hexadecimal or can be omitted:

```
$ lspci -d <Vendor ID>:<Device ID>
```

The following is an example command using the Achronix Vendor ID and a Device ID of 1:

```
$ lspci -d 1b59:0001
```

```
01:00.0 Non-Essential Instrumentation [1300]: Device 1b59:0001 (rev 01)
```

4. If the device has:
 - a. Not enumerated, i.e., the device is not present in the `lspci` output from the previous step, repeat instructions 1 through 3 in this section.
 - b. Enumerated, verify the intended functionality.

 **Note**

On some systems it has been observed that the device might not have enumerated due to the state of the device prior to performing the steps in this section. During system boot, if the device is not programmed (as can be the case during cold boot), the system does not detect the device as active and, therefore, does not provide a necessary clock resource. In this state, since the device has been programmed and rebooted, it should now have the clock resource needed and only requires another iteration of programming and reboot. It has been observed that warm reboot currently causes some registers, such as the BAR size registers, to reset which affects functionality. This issue is to be addressed in a future update. For now, if the device PCIe functionality is invalid, continue with the steps in the following section to ensure functional transactions on the PCIe link.

Reconfiguration of an Enumerated Device

If the device is powered on and has already enumerated, follow these steps to reconfigure the device:

1. Identify the PCI domain number and Bus:Device.Function (BDF) numbers for the endpoint device to be reconfigured and its associated upstream device. The PCI domain number and BDF numbers can be displayed by using the `lspci` command. The numbers are located at the beginning of each PCI device entry of the displayed list. The PCI domain number is the first four hexadecimal digits followed by the BDF number for the device. In the following example, `0000` is the PCI domain number, `00:01.0` is the BDF number for the upstream device, and `01:00.0` is the BDF number for the endpoint device to be reconfigured:

```
$ lspci -D -PP -d <Vendor ID>:<Device ID>

0000:00:01.0/01:00.0 Non-Essential Instrumentation [1300]: Device 1b59:0001 (rev 01)
```

**Note**

By default, the `lspci` command does not display the domain number if the machine only has domain 0. The `-D` flag can be used to always display the PCI domain number. The `-PP` flag displays the path of devices to the PCI device. In this path, the upstream device BDF number precedes the BDF number of the endpoint device. The `-d` flag can be used to show only devices with the specified vendor, device, and class ID. The numbers are given in hexadecimal or can be omitted.

2. Remove the PCI driver module. Removing the driver module also removes the previous device files and, upon rescan, new devices are given an ID starting from 0.

```
$ sudo rmmod <PCI driver>
```

The following example is for removing the BittWare driver, `bwpci`, which is used for the VectorPath accelerator card.

```
$ sudo rmmod bwpci
```

**Note**

If an error message similar to the following appears, it can be ignored. Additionally, the `lsmod` command can be used to confirm that the `bwpci` module is no longer loaded.

```
rmmod: ERROR: Module bwpci is not currently loaded
```

3. Remove the upstream device using the following commands. The device is located in the `/sys/bus/pci/devices/<device>` directory and is identified by its PCI domain and BDF numbers.

```
$ sudo chmod 777 /sys/bus/pci/devices/<PCI domain>:<device BDF>/remove  
$ sudo echo 1 > /sys/bus/pci/devices/<PCI domain>:<device BDF>/remove
```

The following example command uses the PCI domain and BDF numbers from the first step:

```
$ sudo chmod 777 /sys/bus/pci/devices/0000:00:01.0/remove  
$ sudo echo 1 > /sys/bus/pci/devices/0000:00:01.0/remove
```

**Note**

Only removing the endpoint device instead of the upstream device can result in enumeration, but it has been observed that some functionality might be missing.

4. Program the FPGA with the desired bitstream. For more information on programming the FPGA, refer to the [Speedster7t Configuration User Guide \(UG094\)](#).
5. Rediscover the PCI device by performing a rescan of all PCI buses in the system:

```
$ sudo chmod 777 /sys/bus/pci/rescan  
$ sudo echo 1 > /sys/bus/pci/rescan
```

6. Load the PCI driver module.

```
$ sudo modprobe <PCI driver>
```

The following example illustrates loading the BittWare driver for the VectorPath accelerator card.

```
$ sudo modprobe bwpci
```

The device should be enumerated and ready for subsequent PCIe operations using the new programmed bitstream. If the device has not enumerated, contact [Achronix support](#) for assistance.

Revision History

Version	Date	Description
1.0	25 Oct 2022	<ul style="list-style-type: none">Initial Achronix Release.
1.1	02 Mar 2023	<ul style="list-style-type: none">Include usage of Achronix Device Manager for enumeration

Achronix[®]

Data Acceleration

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