Achronix
Data Acceleration

Product Brief

PCIe Accelerator-6D

Board Highlights

PCIe Accelerator-6D Board Features

- HD1000 22-nm FPGA (see below for FPGA details)
- 4 QSFP+ cages for 4× 40G Ethernet or 16 × 10G Ethernet (with breakout connector)
- Full-length PCI Express pluggable form factor: Gen 3 ×8, for 64 Gbps throughput
- Support for twelve DDR3 SODIMMs (2 modules per controller) providing up to 690 Gbps total bandwidth
- Programmable clock sources and clock synthesizers
- Simple USB interface that supports JTAG, CPU and SPI configuration modes
- SPI EEPROM for FPGA configuration

HD1000 Device Features

- 1 million equivalent LUTs (700k programmable LUTs + hardened IP)
- 86 Mb of on-chip memory
- Six hardened DDR3 controllers: up to ×72 wide at 1,600 MT/s each
- 64 SerDes lanes (1 to 10.125 Gbps)
- Two hardened Ethernet MACs each supporting 1× 100GE, 3 × 40GE or 12 × 10GE operation
- Two hardened Interlaken ports each supporting 135 Gbps operation
- Two hardened PCIe controllers – supporting up to Gen3 ×8 operation
- 756 28×28 multiply/accumulate blocks
- 960 programmable user I/O

PCIe Accelerator-6D Board Supporting HD1000

The Achronix PCIe Accelerator-6D Board is the industry's highest memory bandwidth, FPGA-based PCIe add-in card for high-speed acceleration applications. On the card is the Speedster™22i HD1000 FPGA, which connects six independent memory controllers allowing for up to 192 GB of memory and 690 Gbps of memory bandwidth. Each DRAM controller runs at 1,600 MT/s and connects to two SODIMMs allowing for single, dual and quad-rank SODIMM and SORDIMM operation. The board also has four QSFP+ connectors for 10G/40G Ethernet connectivity and supports PCIe Gen3 ×8 operation. Because the controllers for the DDR3, Ethernet and PCIe interfaces are implemented as embedded hard blocks inside the HD1000 FPGA, valuable programmable resources inside the FPGA are not needed to implement these functions. In addition, the embedded hard controllers eliminate the challenge of trying to close timing on designs based on soft controller implementations of high-performance interface protocols.

Sustainable, high-bandwidth functionality is critical for high-performance computing (HPC) applications. High-bandwidth functionality is measured by how fast the system can process data, but is limited by the performance of its slowest interface. The Achronix PCIe Accelerator-6D Board exceeds the system bandwidth of all other FPGA-based PCIe cards with its 160 Gbps of available bandwidth through the four QSFP+ connectors and 690 Gbps of bandwidth to the off-chip DDR3 memory.

High-Speed Interfaces

The Achronix PCIe Accelerator-6D Board supports up to 192 GB memory via two SODIMMs or SORDIMMs attached to for each of the six DDR interfaces, giving a total of twelve sockets. Various combinations of single, dual and quad-rank DDR modules can be used.

There are four 40G-capable QSFP+ cages connected to the Speedster22i HD1000 hardened Ethernet MACs. Users can configure the connectors as four 40G Ethernet interfaces or use a break-out adapter (not included) to enable sixteen independent 10G Ethernet interfaces.

The PCIe Accelerator-6D board comes in a full-height, full-length form factor and supports up to PCIe Gen3 ×1, ×4 and ×8 configurations.

Design Methodology

The HD1000 FPGA functionality is designed using the Achronix CAD Environment (ACE) software development tools. ACE is a full-featured FPGA design environment that delivers best-in-class quality of results for performance, area and compile times.

The ACE design tool suite includes Synplify Pro from Synopsys for RTL synthesis. ACE takes the synthesized design netlist and provides placement, routing, timing analysis, bitstream generation and FPGA configuration. For verification, ACE supports multiple industry-standard simulators and includes SnapShot logic analyzer for real-time, on-chip design debugging. The PCIe Accelerator-6D kit includes a one-year license for both ACE and Synplify Pro for Achronix.

Device Configuration

The HD1000 FPGA and other components on the PCIe Accelerator-6D board are fully controlled from within ACE design software. Users simply plug a USB cable from their computer into the board to do the following:

- Configure the FPGA using JTAG or CPU mode
- Program the SPI EEPROM memories for FPGA configuration
- Use the I^2C interface to program the power regulators and clock synthesizers plus read the temperature sensors, voltages and currents
- Use Achronix's SnapShot real-time design debug tool to monitor signals in the FPGA

Additionally, there are dedicated JTAG and CPU-mode headers on the board that can be used to configure the HD1000 FPGA directly.

Typical Applications

- Data analytics
- Data mining
- Machine learning
- Data center server accelerators
- System modeling
- Packet QoE/QoS monitoring
- Cyber security and DPI
- Test and measurement
- Financial transaction time-critical packet processing

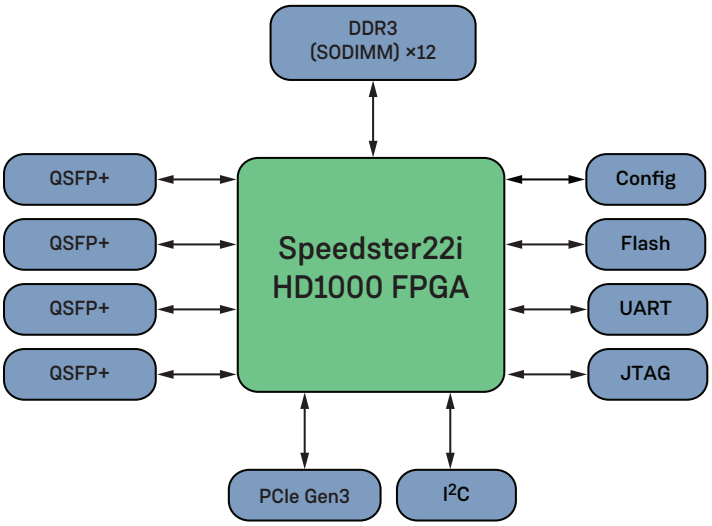
Ordering Information

Ordering code: ACX-KIT-HD1000-PCIE

The kit includes:

- PCIe Accelerator-6D Board
- Two micro-USB cable
- One-year license for ACE design tools
- Multiple system-level reference designs for Ethernet, DDR3 and PCIe operation

The Achronix PCIe Accelerator-6D kit can be ordered through Achronix distribution partners and directly from Achronix. More information is available at the Achronix website: http://www. achronix.com.



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