# PCIe Accelerator-6D Card Quick Start User Guide (UG055)

achronix SEMICONDUCTOR CORPORATION

v1.2

November 09, 2016

# PCIe Accelerator-6D Kit Contents

The following items are included in the PCIe Accelerator-6D Kit:

- One PCIe Accelerator-6D board
- Two micro-USB cable
- One Bitporter pod (if applicable)



#### Figure 1: PCIe Accelerator Card

# **Getting Started**

## Install Achronix CAD Environment (ACE)

Install the latest release of ACE on your system by downloading it from your FTP account with us on our website ( https://secure.achronix.com). Follow instructions to install all related drivers.

## **Setting up the Board**

- 1. The PCIe Accelerator-6D card offers the following primary modes to program the Achronix HD1000 FPGA:
  - a. JTAG via FTDI Connect the USB mini end of provided USB cable to "USB Connector for FTDI" port on the board and the other end of the cable to the standard USB port of the host PC
  - b. JTAG via Bitporter pod Connect the Bitporter (not included) ribbon cable to the JTAG header on Accelerator-6D board. Connect USB mini end of the Bitporter pod to the host system's USB port. Ensure that the Bitporter pod is recognized and powered up (as indicated by the red LED on Bitporter pod).

#### Warning!

Bitporter pod communication can be done via Ethernet or USB. When communicating via USB, DO NOT provide power to the pod through the +5V DC input. Power is provided to the pod via the USB cable. The Bitporter pod should always be powered up before and powered down after the development board to prevent damage and undesired behavior.

For more details about the various programming modes for HD1000 FPGA, refer to the Achronix *Speedster 22i Configuration User Guide* (UG033).

- 2. Connect USB mini end of the second USB cable to the "DCC micro-USB" port on the board and the other end to the standard USB port of the host PC.
- 3. Plug the 12V DC power supply connector end of the main power source into the "12V Power Supply Connector" on the board.

#### Note

If host system's power supply source has multiple taps along the supply cable from where it can be connected to the board, it is recommended to use the tap (supply connector) that is closest to the power supply source. It is also recommended to connect the power supply to both the supply connectors on the board to ensure that the board always has a back-up power supply in case one of them fails.

4. Ensure that the configuration DIP switch SW3000 is set up correctly:

<b>P1</b>	P2	Function	
Off	On	SPI ×1	
On	Off	SPI ×4	
Others		Disable SPI	

#### Note

The board straight out-of-box comes with the switch SW3000 pre-set to "Disable SPI" that allows for programming via JTAG programming mode. Advanced programming modes via the on-board serial Flash and CPU will be made available in a future release of the board user guide.

5. Turn on the power. If everything is connected correctly, the "POWER\_GOOD" LED (DS3000) will turn GREEN.

#### Warning!

Please ensure that nothing is connected to the I2C Header port during board power-up in order to enable the on-board clock chip to correctly boot-up from the on-board EEPROM. You may connect your external I2C device to the I2C header port after board powers-up and the "POWER\_GOOD" LED (DS3000) turns GREEN. This limitation will be fixed in a future revision of the board.

## **Board Operation through ACE**

The PCIe Accelerator-6D board offers two ways of downloading the FPGA bitstream in JTAG mode:

- Bitporter
- Micro-USB (via FTDI)

### **FPGA Bitstream Download using Bitporter**

1. Connect the Biporter Pod to the JTAG header on the board as described in board setup above for programming through JTAG via Bitporter.

2. Switch to "Programming and Debug Perspective" or "HW Demo Perspective" in ACE and configure the JTAG interface such that the "JTAG Programmer Device Type" is set to "Bitporter Pod", and the "JTAG programmer Device Connection" is set to "Auto-Detect JTAG Device".

O ACE - Achronix CAD Environment		
Eile Edit Actions Window Help	no Perspective	
🔗 🔛 🗁 🗸 🖘 🛠 🗈 🛍 🕐 🌮 🖻 🖪 🕼 🚰 🚝	(	Configure JTAG
🅸 SnapShot Debugger 🗣 Download 🛛 🗐 JTAG Browser	► <u></u>	Connection
Select the bitstream file (*.jam) to be used.	O Preterences	
STAPL Design File: Programming and	type filter text	Configure JTAG Connection $\Leftrightarrow \bullet $
Default File from Current Design/Impl Debug Perspective Manual Selection Browse	Configure DCC Conne Configure JTAG Conne Critical Path Diagram	JTAG Programmer Device Type Bitporter Pod  TDI FT2232H
STAPL Actions and Procedures	Floorplanner View Co Floorplanner View Op	JTAG Programmer Device Connection Auto-Detect JTAG Device  Specify JTAG Device Name

Figure 2: ACE Programming and Debug Perspective - Bitporter

- 3. In the HW Demo perspective, configure the DCC interface port name to COM3 and ensure that this matches the COM number for the USB port in the Device Manager settings of the host system under the Control Panel. If not, change the COM number for the USB port to COM3. If board was setup correctly as per the board setup instructions above, the CONFIG\_STATUS LED should be lit.
- 4. Download the board startup design bitstream (/public/Achronix/demos/pac6d\_startup\_design. zip) from the Achronix download site (https://secure.achronix.com). Unzip this file and program the bitstream into the FPGA. When the configuration is complete, the CONFIG\_DONE LED should be lit. Ensure that the user LEDs are blinking.

The board is set-up and operational.

## FPGA Bitstream Download using Micro-USB (via FTDI)

#### Feature Not Available

This feature is temporary unavailable. This feature will be made available in a future release of ACE. Please file a request to support@achronix.com for any inquiries related to ACE software releases and feature availability.

- 1. Connect the USB cable to the micro-USB port on the board as described in the board setup above for programming through JTAG via FTDI.
- 2. Switch to "Programming and Debug Perspective" or "HW Demo Perspective" in ACE and configure the JTAG interface such that the "JTAG Programmer Device Type" is set to "FTDI FT2232H", and the "JTAG programmer Device Connection" is set to "Auto-Detect JTAG Device".

O ACE - Achronix CAD Environment		
<u>File Edit Actions Window H</u> elp		
🧀 🔛 🗁 🛷 🤟 🗈 👔 🦅 😢 🗈 🕈 🚰 🚝 🚝 🚝 HW Demo Per	spective	Configure JTAG
🎋 SnapShot Debugger 🗟 Download 🖾 🗐 JTAG Browser	► É <sup>la</sup>	Connection
▼ STAPL Design File Select the bitstream file (*jam) to be used.	O Preferences	
STAPL Design File:	type filter text	Configure JTAG Connection
Default File from Current Design/Impl Programming and Manual Selection Browse Debug Perspective	Configure DCC Conne Configure JTAG Conne Critical Path Diagram Floorplanner View Co Floorplanner View Op	JTAG Programmer Device Type Bitporter Pod FTDI FT2232H
✓ STAPL Actions and Procedures		JTAG Programmer Device Connection Auto-Detect JTAG Device  Specify JTAG Device Name

Figure 3: ACE Programming and Debug Perspective - FTDI

- 3. In the HW Demo perspective, configure the DCC interface port name to COM3, and ensure that this matches the COM number for the USB port in the Device Manager settings of your system under the Control Panel. If not, change the COM number for the USB port to COM3. If board was setup correctly as per the board setup instructions above, the CONFIG\_STATUS LED should be lit.
- 4. Download the board startup design bitstream (/public/Achronix/demos/pac6d\_startup\_design. zip) from the Achronix download site (https://secure.achronix.com). Unzip this file and program the bitstream into the FPGA. When the configuration is complete, the CONFIG\_DONE LED should be lit. Ensure that the user LEDs are blinking.

The board is set-up and operational.

# Note Refer to the latest version of this document located in the documentation section of the Achronix website using the following link: http://www.achronix.com/wp-content/uploads/2016/10 /PCle\_Accelerator-6D\_Card\_Quick\_Start\_User\_Guide\_UG055.pdf File a request to support@achronix.com for any inquiries or unexpected board behavior.



#### **Achronix Semiconductor Corporation**

2953 Bunker Hill Lane, Suite 101 Santa Clara, CA 95054 USA Phone : 855.GHZ.FPGA (855.449.3742) Fax : 408.286.3645 E-mail : info@achronix.com

Copyright © 2016 Achronix Semiconductor Corporation. All rights reserved. Achronix, Speedcore, Speedster, and ACE are trademarks of Achronix Semiconductor Corporation in the U.S. and/or other countries All other trademarks are the property of their respective owners. All specifications subject to change without notice.

NOTICE of DISCLAIMER: The information given in this document is believed to be accurate and reliable. However, Achronix Semiconductor Corporation does not give any representations or warranties as to the completeness or accuracy of such information and shall have no liability for the use of the information contained herein. Achronix Semiconductor Corporation reserves the right to make changes to this document and the information contained herein at any time and without notice. All Achronix trademarks, registered trademarks, disclaimers and patents are listed at http://www.achronix.com/legal.