PCIe Accelerator-6D Card User Guide (UG074)

Speedster FPGAs

achronix
SEMICONDUCTOR CORPORATION

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Figure 1: ***Achronix PCIe Accelerator-6D Board***

PCIe Accelerator-6D Kit Contents

The Achronix PCIe Accelerator-6D kit contents are as follows:

- One PCIe Accelerator-6D board
- Two micro-USB cable
- PCIe Accelerator-6D Quick Start User Guide
- Achronix CAD Environment (ACE) license

PCIe Accelerator-6D Kit Uses

This PCIe Accelerator-6D board is designed to achieve a number of functions:

- Demonstrate the capabilities of the HD1000 FPGA to potential customers that will ultimately build their own custom hardware.
- Accelerate compute-intensive tasks within a standard PC/server.
- Add Gigabit Ethernet capability to a host (a combination of 10G and 40G ports)
- Provide a debugging platform for internal Achronix use

PCIe Accelerator-6D Board Features

The PCIe Accelerator-6D board offers the industry's highest memory bandwidth between the Speedster22i HD1000 FPGA, which contains 700,000 LUTs, and six independent, dual-slot DDR3 memory interfaces. Each interface can support single, dual, or quad rank functionality. The DDR3 memory configuration supports up to 192 gigabytes of total memory and can run as fast as 1600 MT/s, which equates to 690 Gbps of total memory bandwidth.

The PCIe Accelerator-6D's four QSFP+ modules support either four 40 gigabit Ethernet ports or sixteen 10 Gigabit Ethernet ports using breakout cables giving a total bandwidth of 160 Gbps. The card also supports PCI Express Gen3 by 8, thus providing 64 Gbps bandwidth.

The Accelerator-6D is the perfect platform for building network and compute acceleration applications such as line-rate deep packet inspection, encryption and decryption algorithms; image processing, machine learning and database acceleration.

FPGA

- Achronix 22-nm, AC22iHD1000F53C2

Functional Blocks

- 1 million equivalent LUTs (700k programmable LUTs + hard IP)
- 86 Mb of on-chip memory (82 Mb BRAM, 4 Mb LRAM)
- 756 28 × 28 multiply/accumulate blocks
- 960 programmable user I/O

Network and Communications

- Hard Ethernet MACs: 100GE, 40GE, 10GE
- 64 SerDes lanes (1 to 12.75 Gbps)
- Hard Interlaken ports, each running up to 11.3 Gbps

System

- Hard PCI Express Gen1/2/3 ×1, ×4, ×8
- Hard DDR3 controllers: six ×72 at 1600 MT/s

Board

- PCI Express pluggable form factor
- Three SMP connectors to provide differential and single-ended FPGA external clock
- Twelve DDR3 SO-DIMM socket
- Four 40 GE QSFP module ports
- Power supply modules
- Power-on reset circuitry
- Oscillators/crystals/clock modules and synthesizers
- Power and temperature measurement sensors
- SPI header for flash memory access
- Flash memory for device configuration
- LEDs, switches, headers
- JTAG header for bitstream programming via Bitporter pod and/or access to FPGA internal registers

- Two micro-USB connectors for bitstream programing via FTDI and to allow access to FPGA internal registers via ACE demo command and control (DDC) connection

> **Note**
>
> Component numbers mentioned in this guide refer to PCIe Accelerator-6D Board component or device markings. Board schematics can be made available upon signing an NDA with Achronix.

Achronix CAD Environment (ACE) Software

Achronix provides ACE software together with an Achronix-optimized version of Synplify-Pro from Synopsys (a node-locked or floating version of the license is needed to use the ACE software for development). See PCIe Accelerator-6D Card Development Environment Setup (see page 13) for more details about installation and use.

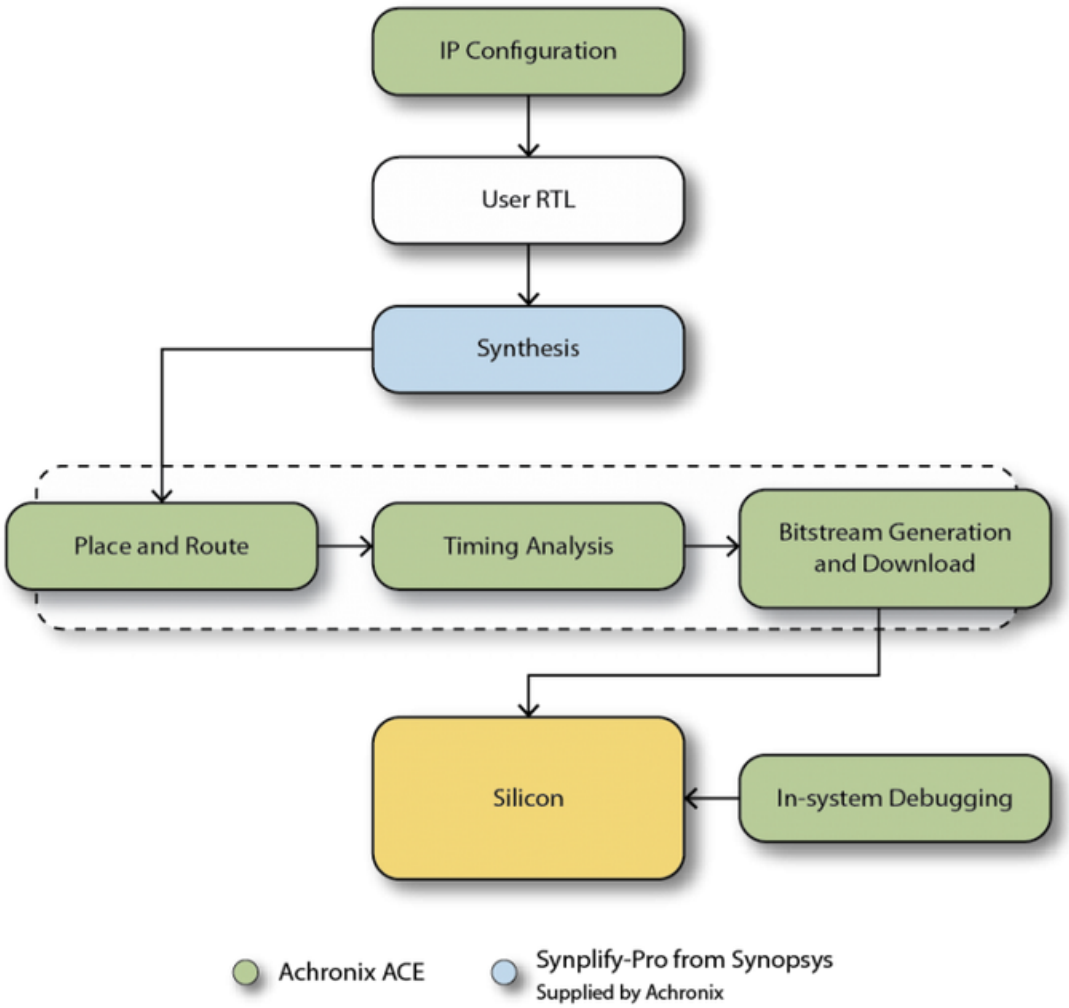

Figure 2: ***ACE Development Environment***

Chapter - 2: General Description

PCIe Accelerator-6D Board

The development board has a PCIe form-factor having a dimension of Length:310 mm × Width:97.5 mm. It also has dedicated power connectors.The figure PCIe Accelerator-6D Board Details (see page 9) below shows the PCIe Accelerator-6D board with many of the key components annotated.

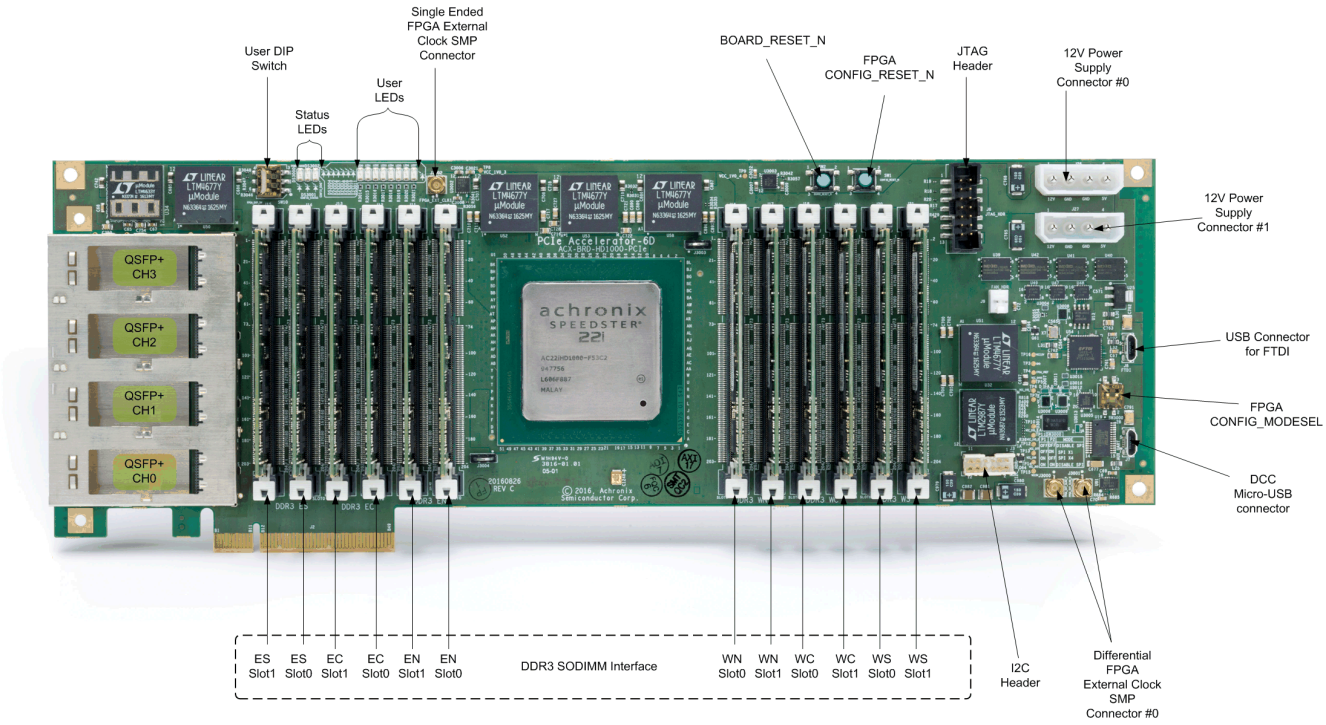

Figure 3: ***PCIe Accelerator-6D Board Details***

User Modes

There are two use modes for this development board, standalone and in-system (plug-in). In both modes, the user must provide power to the board through the dedicated power connectors using an external power supply as shown in the figure below.

Standalone Mode

In this mode, the development board is placed on a bench, with control and data signals coming from the surrounding interfaces, which may include the DIP switches, SMP connectors, I^2C header, Maxim temperature sensor, DCC mcro-USB connector, nicro-USB connector for programming the FPGA over FTDI in JTAG mode, etc.

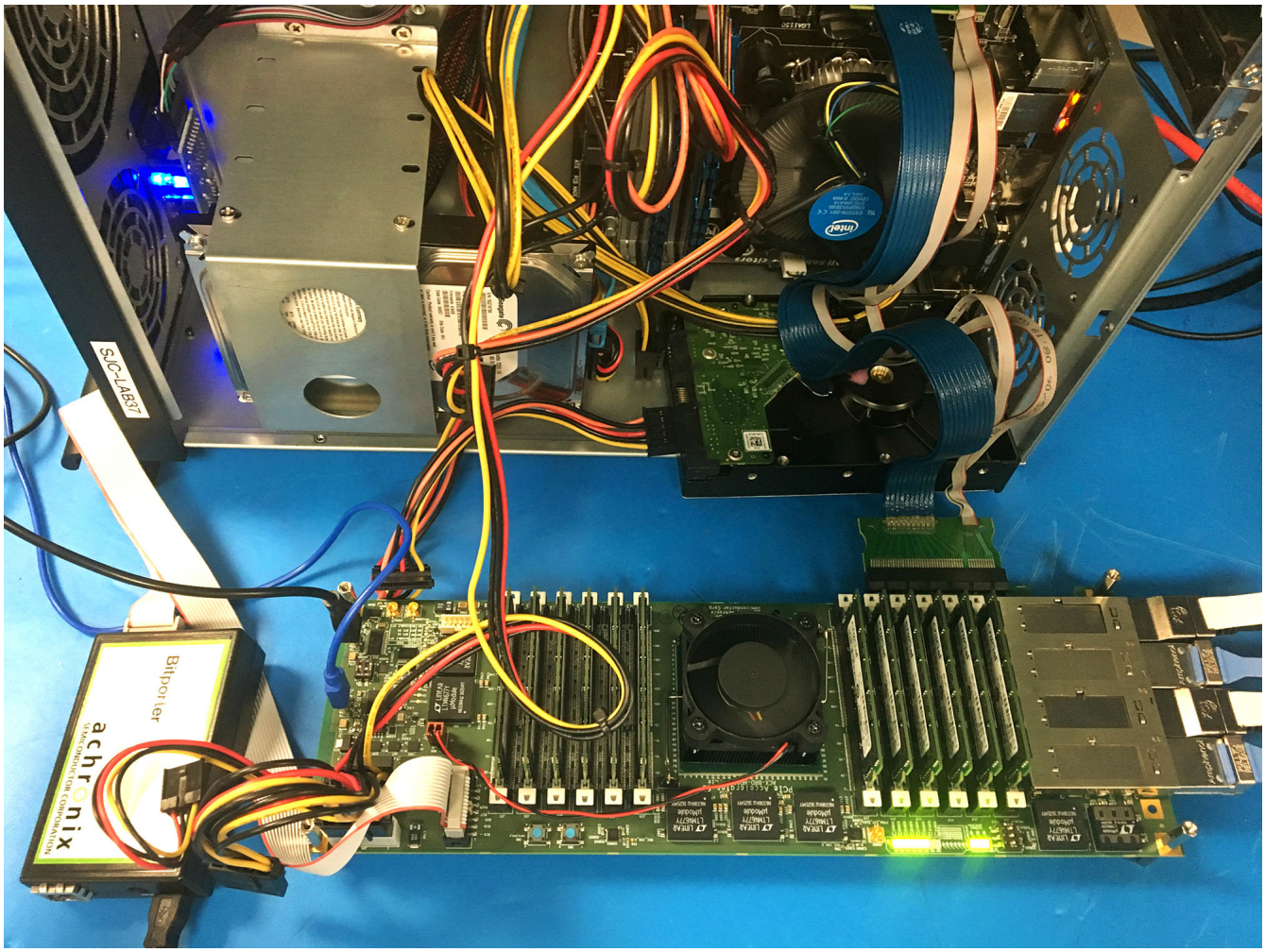

Figure 4: ***PCIe Accelerator-6D Board Connected in Standalone Mode***

In-system (Plug-in) Mode

The PCIe Accelerator-6D board is inserted into a PCIe Gen3 ×8 slot of a PC. In addition to the capabilities highlighted in the standalone mode, data traffic can be supplied over the PCIe interface in this mode, assuming the PCIe interface of the FPGA is configured appropriately. This mode is shown in the figure below:

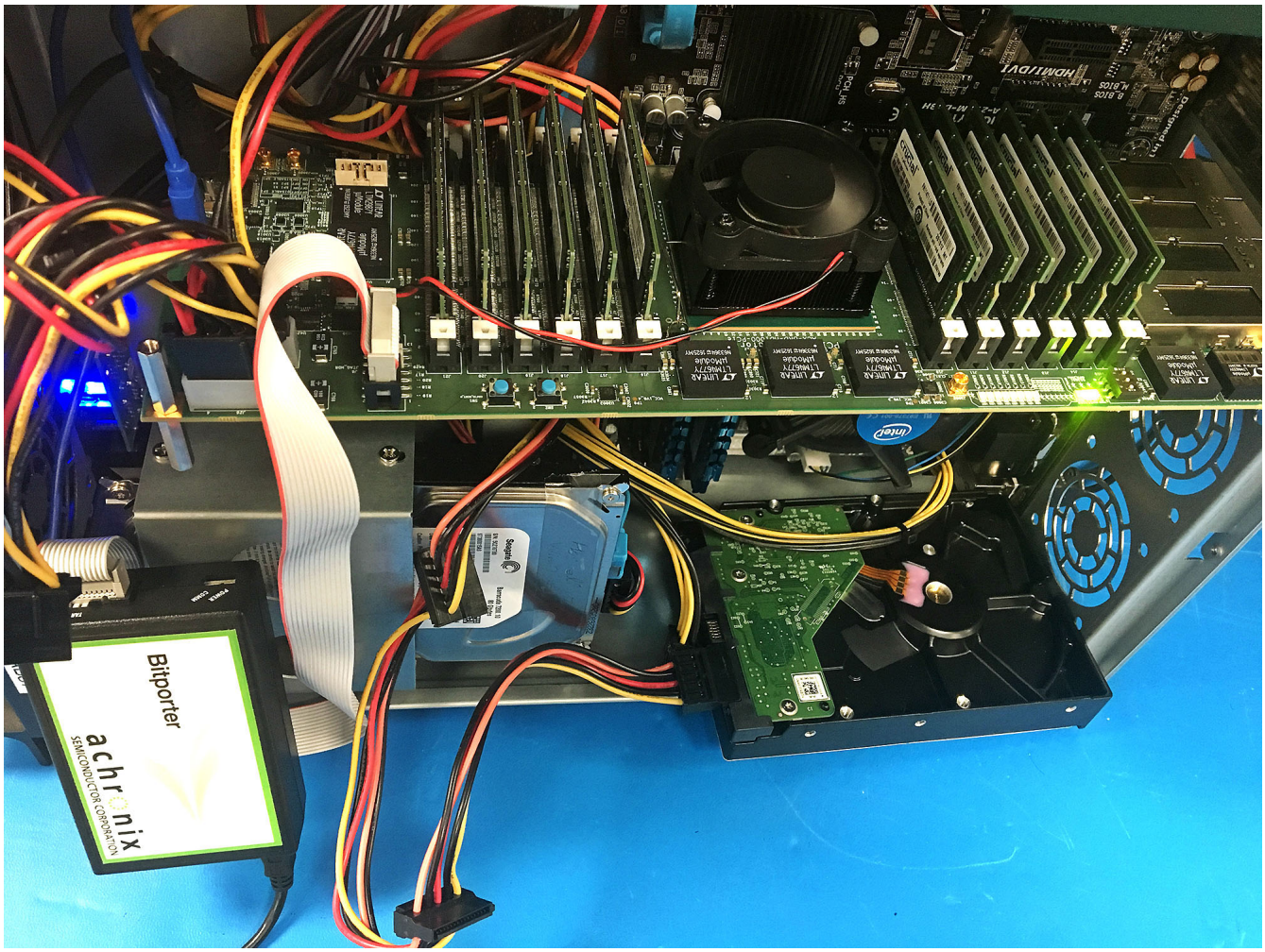

Figure 5: ***PCIe Accelerator-6D Board Connected in In-system Mode***

> **Note**
>
> Power must still be provide to the board via an external power supply rather than the PCIe connector and the dedicated power connectors on the board.

On-Board Memory

The development board has the following memories available for system design.

- Twelve 204-pin DDR3 SO-DIMM connectors to allow for loading of 12 DDR3 SO-DIMMs each of which has a performance of 12.8 Gbps or 1600 MT/s. This memory serves as the primary off-chip memory for all applications, supplementing the on-chip BRAM. This memory also demonstrates the embedded DDR3 controller capability.
- An 512 Mb SPI flash device used to store configuration bitstreams on board.

On-Board Temperature Sensor

The PCIe Accelerator-6D card comes with an on-board Maxim temperature sensor which can be accessed via the I^2C interface to measure the temperature captured by the onchip temperature diode of in the HD1000 FPGA.

Board-Specific Design Issues

The PCIe Accelerator-6D board is optimized for networking and compute acceleration applications. As such, Achronix has configured the SerDes and the I/O at specific pins on the HD1000 device. This configuration must maintain during any changes made to the design hosted in the FGPA. Achronix provides a template for ACE to avoid inadvertent changes to the configuration. The clocking structure implemented on the board must also be maintained during any design changes.

Chapter - 3: Development Environment Setup

Installing Achronix Software (ACE plus Synopsys Synplify Pro) and Licenses

Achronix provides ACE and Achronix's OEM version of Synopsys Synplify Pro licenses for design. *Achronix Software & License User Guide* (UG002) provides detailed information about acquiring and installing ACE and Synplify Pro licenses and software. A download account is required in order to download the software and request a license. Below is a quick summary of steps to install the Achronix software and licenses:

1. From https://downloads.achronix.com download the following files, depending on the host setup:
    a. Windows node locked/Windows client software
    b. Floating (Windows license server)
    c. Linux node locked/Linux client software
    d. Windows node locked/Windows client software
2. Install licenses e-mailed by Achronix on the license server.
3. Modify the license servers for floating licenses only (cases b, c, e, and f)
4. Run the license servers (not needed for case a, Windows node-locked)
5. Set the client machine environment variables
6. Run the software

For more details on Steps 1 through 6 refer to the Achronix Software & License User Guide .

Running ACE

After installation and licensing, run the executable file to start using ACE. For more information about getting started with ACE, refer to *ACE User Guide* (UG001).

Setting up the PCIe Accelerator-6D Board

Depending on the evaluation requirements, choose either the standalone or the in-system (plug-in) mode of operation for the board.

Standalone Mode

The board must be connected the host PC and an external power source. The connections are shown in Figure Standalone Board Connections (see page 14) below.

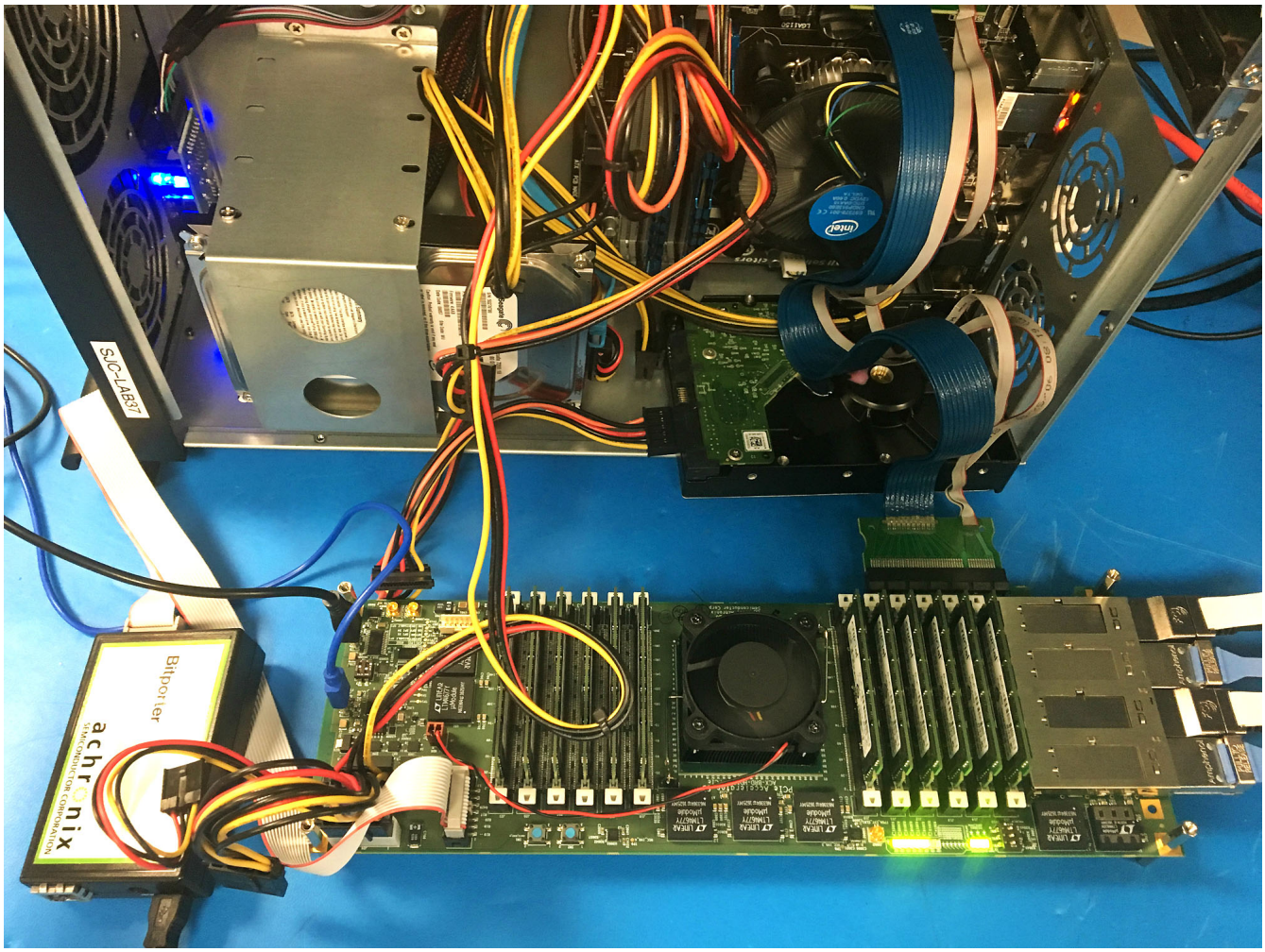

Figure 6: ***Standalone Board Connections***

Connecting the Host PC

Based on the system requirements, the following are the connections needed to the host PC:

1. Connect the supplied micro-USB cable the to the "USB Connector for FTDI" (see figure: *PCIe Accelerator-6D Board Details (see page 9)*) for programming the FPGA and/or accessing HD1000's internal registers via FTDI over JTAG.
2. Connect the second supplied micro-USB cable to the "DCC Micro-USB Connector" (see figure: *PCIe Accelerator-6D Board Details (see page 9)*) for accessing the HD1000's internal registers via DCC.
3. Connect the extended Gen3 ×8 PCIe connector to the PCIe edge connector on the board (see figure: *PCIe Accelerator-6D Board Details (see page 9)*).

Connecting the Power Supply

Although the individual components on the board use different voltage levels, each of these is generated on the board using a single 12V power supply input.

In-system Mode

For in-system mode, plug the Accelerator-6D board into an available PCIe ×8 slot of the host PC. Make sure the adjacent slot is also vacant to accommodate the clearance requirements for the component side of the board. Figure In-System Board Connections (see page 15) shows the connections for this mode.

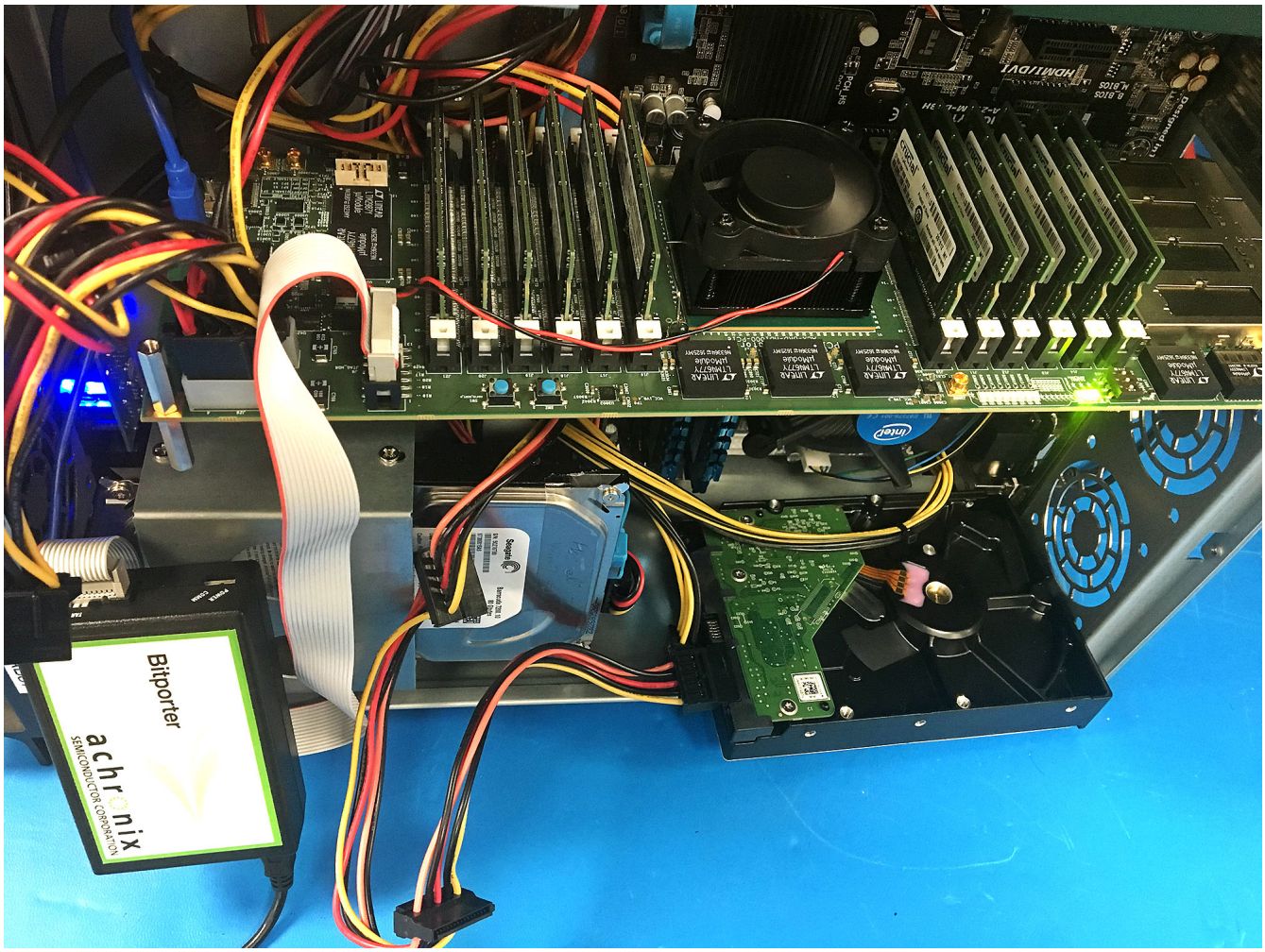

Figure 7: ***In-System Board Connections***

Connecting the Power Supply

Although the individual components on the board use different voltage levels, each of these is generated on the board using a single 12V power supply input. A spare 12V supply connector from the host PC power supply can be used.

Getting started

Power Sequencing

The power sequencing on the board is pre-configured and is controlled by Linear Technology's LTM2987 power system manager. After connecting the power supply and the POWER GOOD LED (DS3000) is steady green, the board is fully powered up and has initialized all the components in the right order.

Initialization

As mentioned above, the power to all devices on the board is controlled by the pre-configured LTM2987 power system manager which acts as the I^2C master initially during power-up. This device then drives and manages the various other LTM switching regulators which provide power to the various power rails of the HD1000 FPGA. Once the board is powered-up, a set of LEDs light. Refer to the PCIe Accelerator-6D Card Quick Start User Guide for details on default power-up behavior.

Following power-up the various clock are then brought up. The clocks on the board come pre-configured and generated by IDT clock device. The various devices on the board can be controlled via the I^2C bus by either the on board HD1000 FPGA or through an external device via the DC1613A I^2C programming connector, either of which can act as the I^2C bus master. After power-up and initialization, the HD1000 becomes the default I^2C bus master.

Downloading a Design

Typically, the following steps are needed to download a design to the board and start debugging an application.

1. Configuring the Board for the Appropriate Bitstream Source (see page 16)
2. Connecting the Host PC (see page 14) and Running the application

The following sources are currently supported for the FPGA bitstream on this board:

- Bitstream download via JTAG using the on-board FTDI device its corresponding micro-USB port using the provided micro-USB cable which connect to the host PC.
- Bitstream download via JTAG using a Bitporter pod which connects to the host PC.
- Bitstream programming using the on-board flash SPI (×1, ×4) memory and CPU programming mode (may be made available in future release).

Configuring the Board for the Appropriate Bitstream Source

The board is pre-configured with switch SW3000 set to "Disable SPI" to accept bitstreams from the JTAG interface. The following is SW3000 switch configuration for the various programming interface modes:

Table 1: ***SW3000 Programming Interface Switch Connections***

P1	P2	Function
Off	On	SPI ×1
On	Off	SPI ×4
Others		Disable SPI

Connecting the Board to the Host PC and Running the Application

When programming via the JTAG interface:

1. **Via FTDI** – connect the micro-USB cable to the "USB Connector for FTDI" (see figure: *PCIe Accelerator-6D Board Details (see page 9)*) port on the board and the other end to the USB port of the host PC.
   Via Bitporter – connect the Bitporter pod using the ribbon cable to the "JTAG Header" (see figure: *PCIe Accelerator-6D Board Details (see page 9)*). Connect the USB end of Bitporter pod to USB port of the host PC.
2. Power up the board.
3. Run ACE and switch to "Programming and Debug Perspective" or "HW Demo Perspective" to program the bitstream.

Once the FPGA is programmed and the CONFIG_DONE LED light is green, the configuration has successfully completed, and the FPGA has transitioned to user mode. At this point, run any application as desired.

For more details refer to the board PCIe Accelerator-6D Card Quick Start User Guide and Bitstream Programming and Debug Interface User Guide.

Chapter - 4: Interfaces

There are various interfaces available on the HD1000 FPGA and the Accelerator-6D board. These interfaces are discussed in more detail in the following sections:

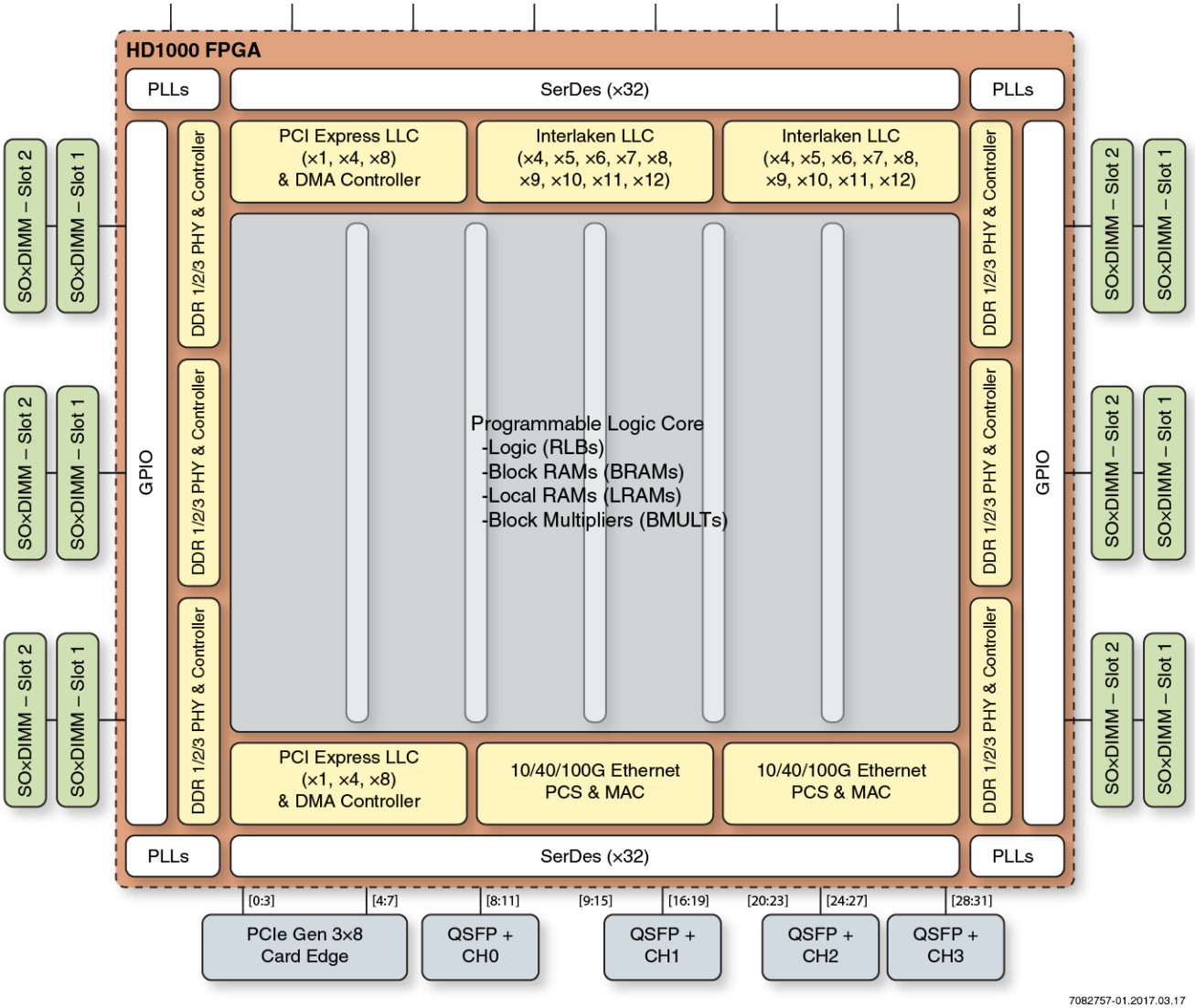

Figure 8: ***PCIe Accelerator-6D Card Interfaces***

Networking and Communications Interface

The four QSFP ports provide a primary high-speed networking data interface for the board, enabling the 10G /40G capabilities of HD1000. For the data path, the four 40G QSFP ports together provide a total duplex bandwidth of 320 Gb/s bandwidth (160 Gb/s transmit and 160 Gb/s receive). These ports can used to support any of of the following Ethernet data rates:

1. 1 × 100G (10 × 10G with split-out cables)
2. 4 × 40G (4 QSFP transceiver modules)
3. 16 × 10G (with split-out cables)

The four-port QSFP cage is directly connected to 16 bidirectional 12.5 G SerDes lanes. These are designated in quads as SerDes CH0 [8:11], CH1 [16:19], CH2 [24:27], CH3 [28:31] as shown in the figure above. Table below shows the pin assignment for the QSFP interface to the HD1000 SerDes pin.

Table 2: ***Accelerator-6D Rev C QSFP Interface Pins***

QSFP Module Pin Name	QSFP CH No./HD1000 SerDes No.	Pin on HD1000 (U1)
RIGHT_TX1_N	**CH 0** 8 - 11	B19
RIGHT_TX1_P		C19
RIGHT_TX2_N		A20
RIGHT_TX2_P		B20
RIGHT_TX3_N		C21
RIGHT_TX3_P		B21
RIGHT_TX4_N		B22
RIGHT_TX4_P		A22
RIGHT_RX1_N		E19
RIGHT_RX1_P		F19
RIGHT_RX2_N		F20
RIGHT_RX2_P		G20
RIGHT_RX3_N		E21
RIGHT_RX3_P		F21
RIGHT_RX4_N		F22
RIGHT_RX4_P		G22

QSFP Module Pin Name	QSFP CH No./HD1000 SerDes No.	Pin on HD1000 (U1)
R_MID_TX1_N	**CH 1** 16 - 19	C27
R_MID_TX1_P		B27
R_MID_TX2_N		B28
R_MID_TX2_P		A28
R_MID_TX3_N		C29
R_MID_TX3_P		B29
R_MID_TX4_N		B30
R_MID_TX4_P		A30
R_MID_RX1_N		E27
R_MID_RX1_P		F27
R_MID_RX2_N		F28
R_MID_RX2_P		G28
R_MID_RX3_N		E29
R_MID_RX3_P		F29
R_MID_RX4_N		F30
R_MID_RX4_P		G30
L_MID_TX1_N	**CH 2** 24 - 27	C35
L_MID_TX1_P		B35
L_MID_TX2_N		B36
L_MID_TX2_P		A36
L_MID_TX3_N		C37
L_MID_TX3_P		B37
L_MID_TX4_N		B38
L_MID_TX4_P		A38

QSFP Module Pin Name	QSFP CH No./HD1000 SerDes No.	Pin on HD1000 (U1)
L_MID_RX1_N	**CH 2** 24 - 27	E35
L_MID_RX1_P		F35
L_MID_RX2_N		F36
L_MID_RX2_P		G36
L_MID_RX3_N		E37
L_MID_RX3_P		F37
L_MID_RX4_N		F38
L_MID_RX4_P		G38
LEFT_TX1_N	**CH 3** 28 - 31	C39
LEFT_TX1_P		B39
LEFT_TX2_N		B40
LEFT_TX2_P		A40
LEFT_TX3_N		C41
LEFT_TX3_P		B41
LEFT_TX4_N		B42
LEFT_TX4_P		A42
LEFT_RX1_N		E39
LEFT_RX1_P		F39
LEFT_RX2_N		F40
LEFT_RX2_P		G40
LEFT_RX3_N		E41
LEFT_RX3_P		F41
LEFT_RX4_N		F42
LEFT_RX4_P		G42

System Interfaces

The Accelerator-6D board has the following system interfaces:

- PCI Express (see page 22)
- USB (see page 24)
- JTAG (see page 25)

PCI Express

A PCIe connector is available for plugging the card into a host PC where the data is provided over the interface. The Gen 3, ×8 interface supports 2 ×64 Gb/s throughput (64 Gb/s receive, 64 Gb/s transmit). The figure above shows the dedicated PCIe pins on the HD1000, designated SerDes Bottom 0 – 7 in the figure. The table below shows the pins on the HD1000 and their connections to the PCIe edge connector.

> **Note**
>
> Power is not supplied to the board via the PCIe connector.

Table 3: ***HD1000 PCIe Edge Connector Mapping***

Signal Name	SerDes No	Pin on HD1000 (U1)	Pin on PCIe ×8 Finger (J2)
PCIE0_PERST_N_LT	–	P15	A11 via U33
PCIE0_RX0_P	0	G18	B14
PCIE0_RX0_N		F18	B15
PCIE0_TX0_P		A18	A16
PCIE0_TX0_N		B18	A17
PCIE0_RX1_P	1	F17	B19
PCIE0_RX1_N		E17	B20
PCIE0_TX1_P		B17	A21
PCIE0_TX1_N		C17	A22
PCIE0_RX2_P	2	G16	B23
PCIE0_RX2_N		F16	B24
PCIE0_TX2_P		A16	A25
PCIE0_TX2_N		B16	A26

Signal Name	SerDes No	Pin on HD1000 (U1)	Pin on PCIe ×8 Finger (J2)
PCIE0_RX3_P	3	F15	B27
PCIE0_RX3_N		E15	B28
PCIE0_TX3_P		B15	A29
PCIE0_TX3_N		C15	A30
PCIE0_RX4_P	4	G14	B33
PCIE0_RX4_N		F14	B34
PCIE0_TX4_P		A14	A35
PCIE0_TX4_N		B14	A36
PCIE0_RX5_P	5	F13	B37
PCIE0_RX5_N		E13	B38
PCIE0_TX5_P		B13	A39
PCIE0_TX5_N		C13	A40
PCIE0_RX6_P	6	G12	B41
PCIE0_RX6_N		F12	B42
PCIE0_TX6_P		A12	A43
PCIE0_TX6_N		B12	A44
PCIE0_RX7_P	7	F11	B45
PCIE0_RX7_N		E11	B46
PCIE0_TX7_P		B11	A47
PCIE0_TX7_N		C11	A48
SERDES_BOT_REFCLK_0_P	–	M25	A13
		M26	
		J25	
		J26	

Signal Name	SerDes No	Pin on HD1000 (U1)	Pin on PCIe ×8 Finger (J2)
SERDES_BOT_REFCLK_0_N	–	N25	A14
		N26	
		K25	
		K26	

USB (J7, J8)

There are two USB connectors on the board, J7 and J8.

The USB (J7) port can be used to communicate between the HD1000 FPGA and the host PC vial an an on-board auxiliary UART FTDI chip (U19), which provides a USB to asynchronous serial data transfer interface. The user design may use this along with the serial bus (sBus) interface on HD1000 FPGA to enable designers to communicate with the internal registers in the Ethernet, SerDes, PCIe, Interlaken, and DDR3 hard IP. For more details on the sBus interface, refer to the Speedster22i sBus Interface User Guide. The table below shows the connection form the USB port to HD1000 FPGA via the auxiliary UART FTDI FT232RL-REEL.

Table 4: ***Accelerator-6D Rev C USB (J7) Interface Connections HD1000 (U1)***

USB Connector (U54)		Auxiliary UART (U19)		HD1000 (U1)	
Signal Name	**Pin**	**Signal Name**	**Pin**	**Signal Name**	**Pin**
D+	3	USB_D_P	15	FPGA_UART_TX	AC42
D-	2	USB_D_N	16	FPGA_UART_RX	AC43

The second USB (J8) port is used for programming the bitstream and communicating with HD1000 via a USB to multipurpose UART FTDI device (U54). FPGA bitstream programming via this FTDI port enable programming for the HD1000 FPGA using JTAG or SPI interfaces of HD1000. For further detail on programming via FTDI, refer to Downloading a Design (see page 16).

Alternatively, the user can also use this USB (J8) port to communicate with the internal registers in the Ethernet, SerDes, PCIe, Interlaken, and DDR3 hard IP via FTDI using the HD1000 JTAG interface. The table below shows the connections from the USB port to FTDI FT2232HQ-REEL (U54).

Table 5: ***Accelerator-6D Rev C USB (J8) Interface Connections to FTDI FT2232HQ-REEL (U54)***

USB Connector (J8)		FTDI FT2232HQ-REEL (U54)	
Signal Name	**Pin**	**Signal Name**	**Pin**
D+	3	DP	2
D-	2	DM	3

JTAG (J6)

JTAG interface (J6) provides access to the JTAG interface pins on the HD1000. The header can be seen in figure: PCIe Accelerator-6D Board Details (see page 9). You can use this information for further debug, development or application actions.This JTAG header also serves as an alternate bitstream programming interface for HD1000 using a Bitporter pod (the Bitporter pod is not provided as a part of the Accelerator-6D kit). For more details, refer to the Bitstream Programming and Debug Interface User Guide.

The signal pins for the 14-pin JTAG header are listed in table below.

Table 6: ***Accelerator-6D Rev C JTAG Header (J6) Pins***

JTAG Header (J6)		Connection		
Signal	**Pin**	**Through**	**Signal Name**	**HD1000 (U33) Pin**
JTAG_TRST_N	1	U48	FPGA_JTAG_TRST_N	L16
JTAG_TMS	7		FPGA_JTAG_TMS	J19
JTAG_TCK	9		FPGA_JTAG_TCK	J13
JTAG_TDI	3		FPGA_JTAG_TDI	K17
JTAG_TDO	5	N/A	FPGA_JTAG_TDO	K16

Memory Interface

SO-DIMM Sockets (J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21)

The Accelerator-6D board has twelve standard 204-pin DDR3 ×72 bit ECC SO-DIMM sockets (J10 through J21), with two per each of the six available DDR3 hard IP controllers on the HD1000 FPGA. These SODIMM sockets can be used to load 12 DDR3 ECC SODIMMs of up to 16 GB each to give a total of 192 gigabytes of on board memory. With the maximum supported bandwidth of 1600MT/s per 16 GB SODIMM, the 12 DIMMs operating in full capacity can provide up to 690 Gbps of total memory bandwidth.

The figure below shows the HD1000 DDR3 controller to SODIMM socket mapping for the six controllers (two slots per DDR3 controller) located on southeast (ES), center east (EC), northeast (EN), southwest (WS), center west (WC) and northwest (WN) of HD1000 FPGA. The HD1000 drives the memory signals using dedicated GPIO. Achronix provides an ACE template to correctly allocate these I/O pins. For the complete list of DDR3 signal mappings to HD1000 FPGA pin, refer to *Speedster22i HD1000 Pin Table* available in the documents section of the Achronix website.

Note

The kit does not ship with the above reference SODIMMs.

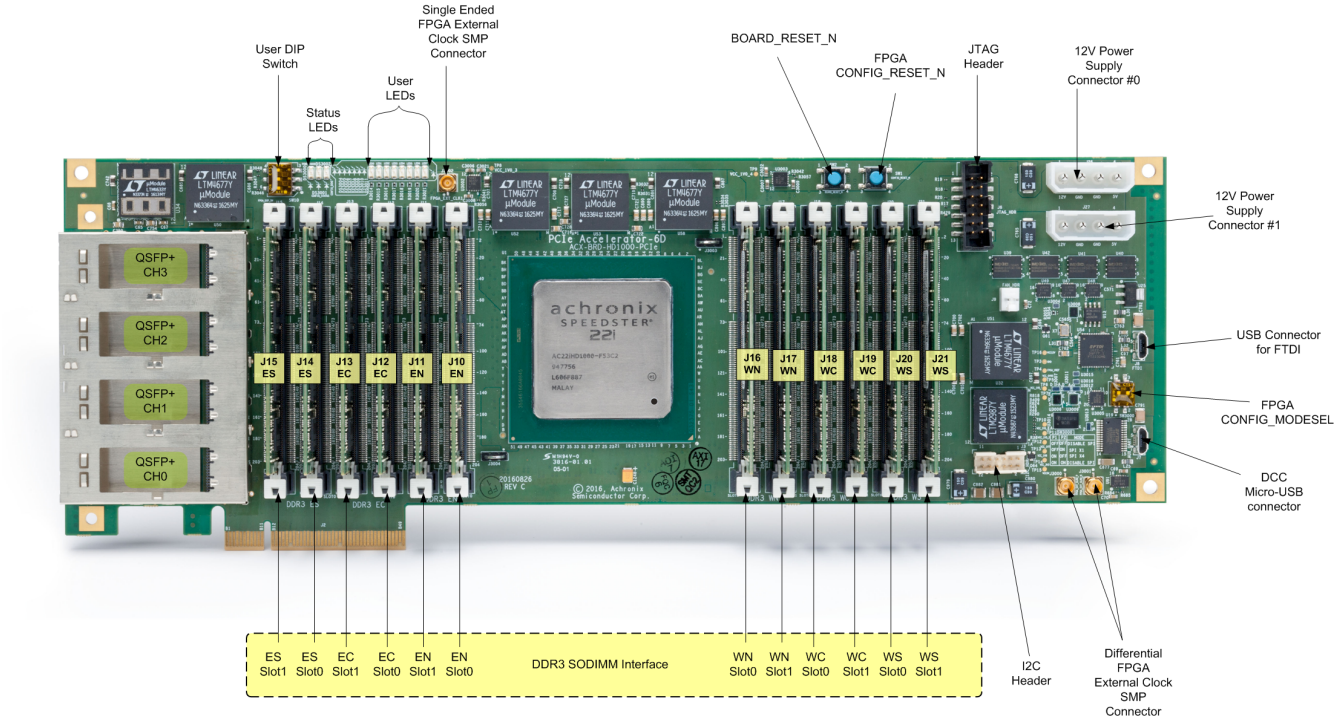

Figure 9: ***Accelerator-6D Rev C SODIMM sockets***

The following memory configurations are supported:

- Single rank - single slot
- Dual rank - single slot
- Dual rank - dual slot

User Interfaces

The following interfaces can be used to configure and drive the board, connect cables, review status of the board, and perform other functions related to development work.

- FTDI CLI (see page 27)
- Bitporter CLI (see page 27)
- ACE GUI (see page 27)
- SMP Connectors (see page 29)
- LEDs (see page 30)
- Switches (see page 31)

FTDI CLI

The PCIe Accelerator-6D's on-board FTDI solution allows for programming and debug of HD1000 FPGA using a command-line interface via a micro-USB connector (J8). The FTDI FT2232H device's multi-protocol synchronous serial engine (MPSEE) is configured for single-chip USB-to-JTAG communication, thus providing a direct interface to the host PC via a USB 2.0 (compatible with USB1.0/USB3.0) interface. Execute `acx_stapl_player.exe` from a command-line interface (CLI) window on the development PC to download and configure the HD1000 directly via USB. For more details on programming the HD1000 FPGA using the Achronix STAPL Player, refer to the *Bitstream Programming and Debug Interface User Guide* (UG004) - Chapter 4: Using the Achronix STAPL Player.

Bitporter CLI

As mentioned earlier, the HD1000 FPGA can be programmed via the JTAG interface using a Bitporter pod. If a Bitporter pod is connected to the JTAG interface (J6) and the SW30000 switch is set to use the JTAG interface as per the table, SW3000 Programming Interface Switch Connections (see page 17), use the command line interface to configure, program and debug the HD1000. Execute `acx_stapl_player.exe` from a command line interface (CLI) window on the development PC to download and configure the HD1000. For more details on programming the HD1000 FPGA using the Achronix STAPL Player, refer to the Bitstream Programming and Debug Interface User Guide - Chapter 4: Using the Achronix STAPL Player.

> **Note**
>
> Care must be taken when powering up the Bitporter pod and the development board. Refer to the Bitstream Programming and Debug Interface User Guide for more details.

ACE GUI

Besides programming the HD1000 FPGA, the ACE GUI can also be used for communicating with the board. The following figures show various ACE GUI perspectives for bitstream programming and communication with the board.

- Figure ACE GUI for Bitstream Programming (see page 28) shows a screenshot of the `acx_stapl_player.exe` file executed from the ACE “Download” View.
- Figure ACE GUI for Register Access via JTAG (see page 28) shows a screenshot of the JTAG Browser perspective using which the user can access all the hard-IP registers.
- Figure ACE GUI for Real-time Design Debug (see page 29) shows a screenshot of the Snapshot perspective through which one can evaluate the signals of a user's design in real-time. For more details please refer to the Snapshot User Guide.
- Figure ACE GUI for Hardware Demo (see page 29) shows a screenshot for Hardware Demo perspective which is TCL base UI for control and monitoring of hardware demo and reference designs.

For more details, please refer to the ACE User Guide.

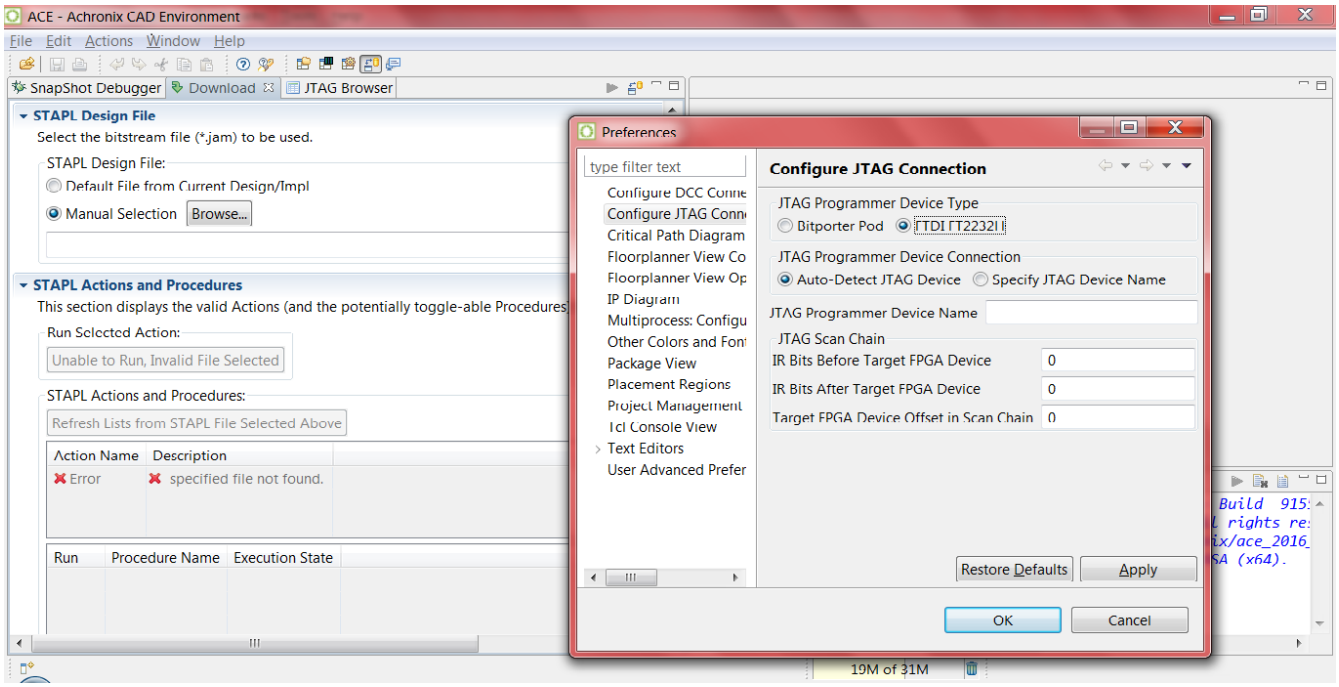

Figure 10: *ACE GUI for Bitstream Programming*

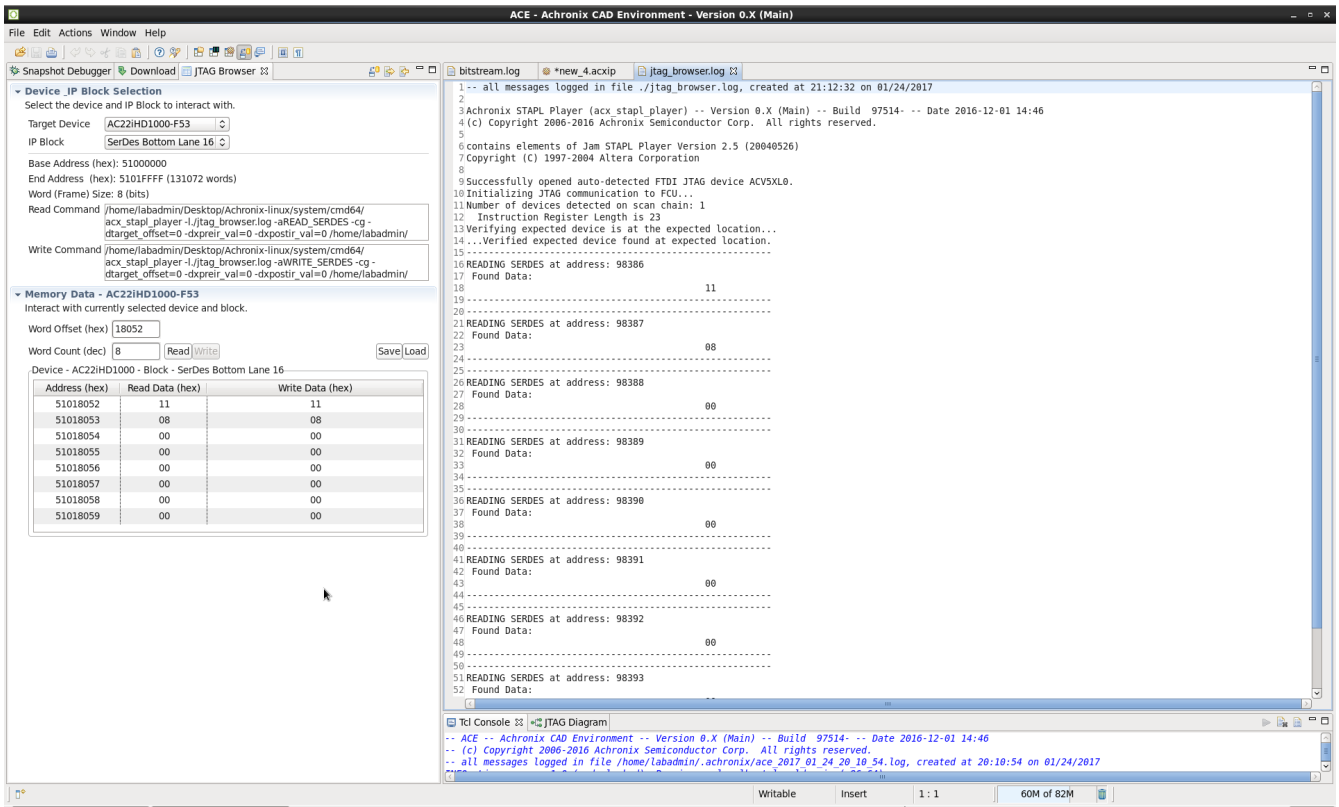

Figure 11: *ACE GUI for Register Access via JTAG*

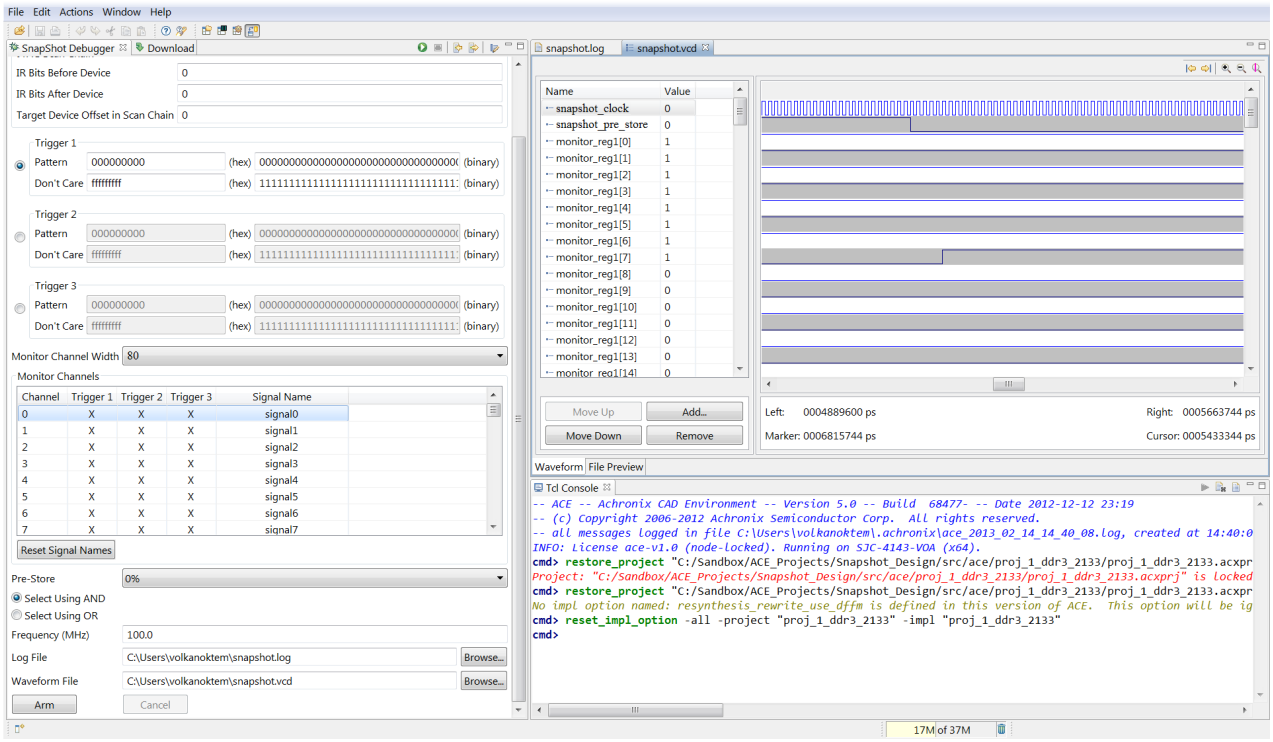

Figure 12: *ACE GUI for Real-time Design Debug*

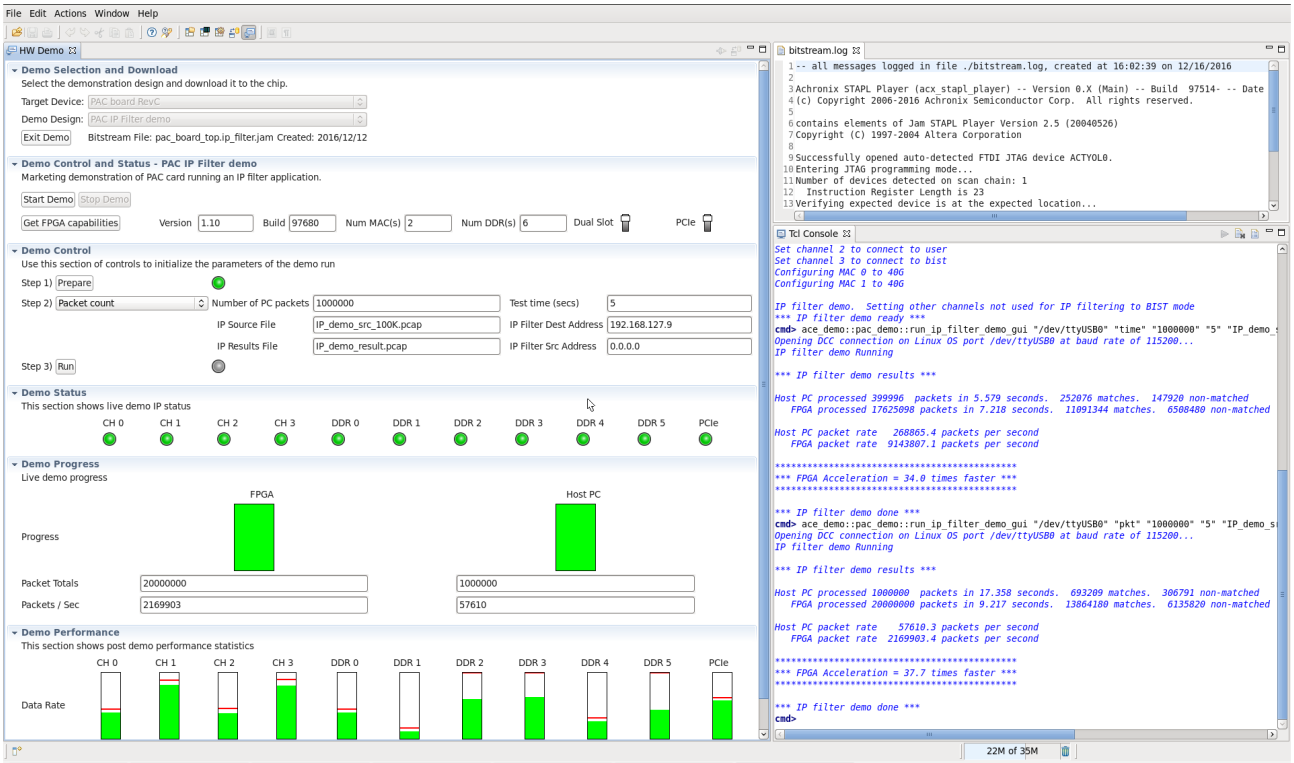

Figure 13: *ACE GUI for Hardware Demo*

SMP Connectors

There are three SMP connectors on the board that can be used for various clocking functions (see the figure, PCIe Accelerator-6D Board Details) (see page 9). These are connected to the HD1000 as shown in table below.

Table 7: ***SMP Connectors Mapping to HD1000 Pins***

Signal	Pin on HD1000 (U1)	Connector	
		SMP	Function
FPGA_EXT_CLK0_P	P17	J3000	Differential FPGA external clock
FPGA_EXT_CLK0_N	P16	J3001	
FPGA_EXT_CLK1	AV37	J3002	Single-ended FPGA external clock

LEDs

There are eleven LEDs on the board. Three are dedicated to provide status information while the rest are user-programmable. The following table lists all the LEDs, their function and connection to HD1000 FPGA.

Table 8: ***LED Connections***

LED	Function	Net Name	Component/Pin
DS3000	Board Power Good indicator	POWR_GOOD_3V3	U3014/F6
DS3001	Configuration status indicator	FTDI_CONFIG_STATUS	U3014/F5
DS3002	Configuration done indicator	FTDI_CONFIG_DONE	U3014/G6
DS3004	User defined	FPGA_LED0	U1/AV38
DS3005		FPGA_LED1	U1/AY37
DS3006		FPGA_LED2	U1/AY38
DS3007		FPGA_LED3	U1/BB14
DS3008		FPGA_LED4	U1/AV14
DS3009		FPGA_LED5	U1/P18
DS3010		FPGA_LED6	U1/P37
DS3011		FPGA_LED7	U1/M38

Switches

There are two push-button switches (SW1 and SW2) and two DIP switches (SW10 and SW3000) on the board (see the figure, PCIe Accelerator-6D Board Details) (see page 9). The following table lists the switches and their function:

Table 9: *Accelerator-6D Switches*

Switch	Type	Description
SW1	Push button	HD1000 FPGA configuration reset switch which will reset/erase the programmed FPGA bitstream. Once pressed, the user will have to re-program the FPGA with the desired bitstream.
SW2		Board reset switch which allows for a manual reset to be provided to the FPGA via a GPIO.
SW10	DIP	User DIP switch available for the user to set the desired functionality for their design.
SW3000		The configuration mode select switch to allow the user to choose between programming the HD1000 FPGA via JTAG or SPI.

Miscellaneous Interfaces

The PCIe Accelerator-6D board has a Linear DC1613A USB to I^2C pod connector interface which is a 12-pin I^2C header (J3) that allows for communication over the I^2C bus to all the various devices on the board. With this interface, the DC1613A pod can control/monitor various voltages, power and current of all the power rails on the board which are driven by their power controller and switching regulator ICs on-board. In addition, this interface can also be used to communicate via the I^2C bus to various devices such as the QSFP transceivers (U116, J5), IDT's 8T49N287 clock frequency synthesizer IC (U12) and Maxim's MAX6642 temperature measurement IC (U31) to measure HD1000 FPGA temperature on the board. For the full device I^2C map, refer to Appendix B: Miscellaneous Diagrams and Figures (see page 36) .

Table 10: *I^2C Header (J3) Pin Connections*

Pin	Net Name
Pin 1	–
Pin 2	SDA_LT
Pin 3	GND
Pin 4	SCL_LT
Pin 5	VCC_3V3_LT
Pin 6	–
Pin 7	–

Pin	Net Name
Pin 8	–
Pin 9	–
Pin 10	GND
Pin 11	–
Pin 12	–

Chapter - 5: PCIe Accelerator-6D Card Clocking

The Accelerator-6D board has an on-board IDT frequency synthesizer U12 (8T49N287) which provides the necessary reference clocks to the HD1000 FPGA PLL clock banks on the four corners and the bottom select SerDes which connect to the four QSFP ports. This frequency synthesizer has been pre-programmed to generate two sets of clocks:

- Four 100 MHz 1.8V LVCMOS single-ended clocks for the HD1000's four PLL clock banks that are on the NW, NE, SW and SE corners.These clocks help the on-chip PLL to generate the necessary frequencies required to implement the system-level functions. For more details on HD1000 clock bank PLLs and clocking architecture, refer to the Speedster22i Clock and Reset Networks User Guide (UG027).
- Three 156.26 MHz 3.3V LVPECL differential clocks provide the SerDes PMA reference clocks to HD1000's bottom four groups of four SerDes lanes each (bottom SerDes CH0 [8:11], CH1 [16:19], CH2 [24:27], CH3 [28:31). These connect to the four QSFP ports on the board. See figure, PCIe Accelerator-6D Card Interfaces, (see page 18) for details.

The Accelerator-6D board also has three SMP connectors (J3000, J3001, J3002) that allow the user to provide differential and single-ended FPGA reference clocks via an external clock source. Refer to section SMP Connectors (see page 29) in PCIe Accelerator-6D Card Interfaces (see page 18) for details.

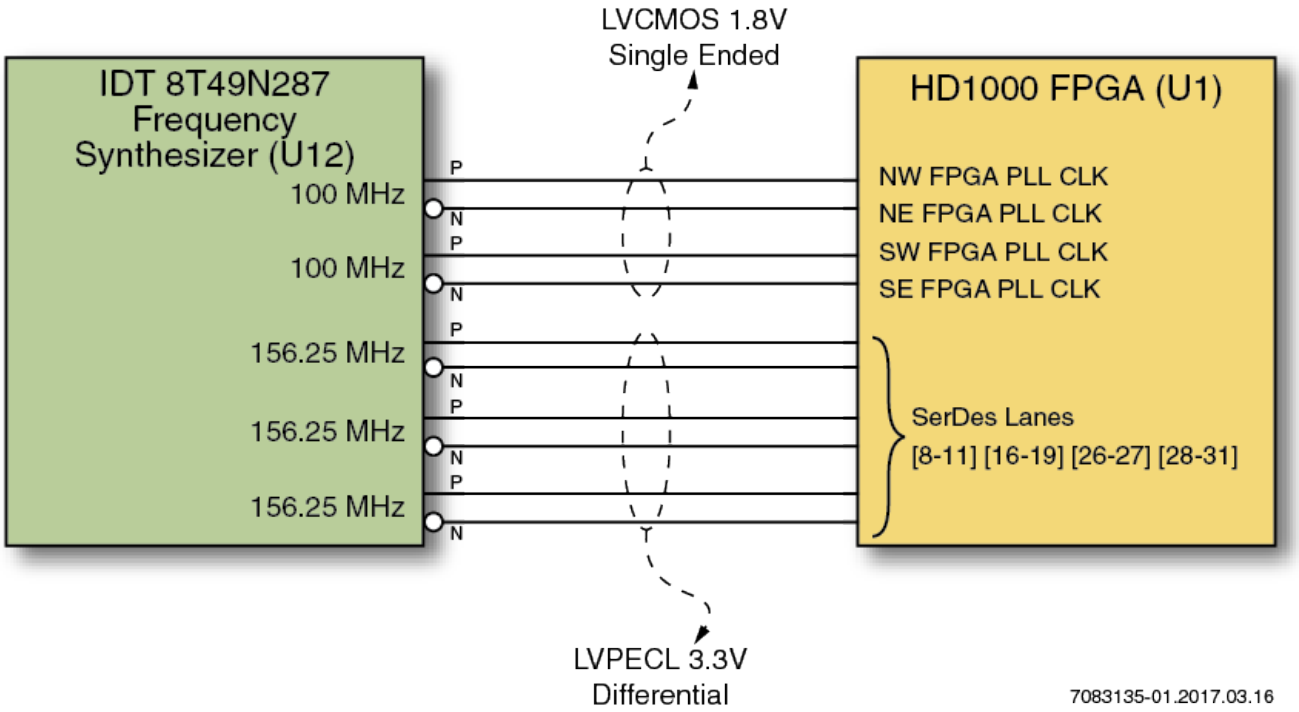

Figure 14: ***PCIe Accelerator-6D Rev C Board Clocking***

Appendix: Board Power Supplies

Component (Component Number)	Power Rail	Power Regulator (Component Number)	V_{IN} (V)	V_{OUT} (V)
HD1000 FPGA (U1)	VCC_1V0_1	LTM4677 (U52)	12	1
	VCC_1V0_2 (a)	LTM4677 (U53)	12	1
	VCC_1V0_2 (b)	LTM4677 (U58)	12	1
	VCC_1V5_2 (DDR_VDD)	LTM4677 (U51)	12	1.5
	VCC_1V5_1 (DDR_VDD)	LTM4677 (U50)	12	1.5
	VCC_3V3	LTM4633 (U34)	5	3.3
	VCC_1V8	LTM4633 (U34)	5	1.8
	VCC0V95	LTM4633 (U34)	5	0.95
	VCC_1V0_3 (VDDA_NOM_E)	LT3083 (U3002)	1.5	1
	VCC_1V0_4 (VDDA_NOM_W)	LT3083 (U3003)	1.5	1
	VCC_1V7	LT3022 (U91)	3.3	1.7
	FPGA_VREF	LT3020 U92)	1	0.762
DDR3 SODIMM EC Slot 1 (J13) / Slot 0 (J12)	DDR_EC_VREF/VTT	LTC3617 (U5)	5	0.75
DDR3 SODIMM EN Slot 1 (J11) / Slot 0 (J10)	DDR_EN_VREF/VTT	LTC3617 (U4))	5	0.75
DDR3 SODIMM ES Slot 1 (J15) / Slot 0 (J14)	DDR_ES_VREF/VTT	LTC3617 (U6)	5	0.75
DDR3 SODIMM WC Slot 1 (J18) / Slot 0 (J19)	DDR_WC_VREF/VTT	LTC3617 (U2)	5	0.75
DDR3 SODIMM WN Slot 1 (J16) / Slot 0 (J17)	DDR_WN_VREF/VTT	LTC3617 (U7)	5	0.75

Component (Component Number)	Power Rail	Power Regulator (Component Number)	V_{IN} (V)	V_{OUT} (V)
DDR3 SODIMM WS Slot 1 (J20) / Slot 0 (J21)	DDR_WS_VREF/VTT	LTC3617 (U3)	5	0.75
Heatsink Fan Header (J9)	Heatsink Fan	F-5010HH12B III	12	NA

Appendix: Miscellaneous Diagrams and Figures

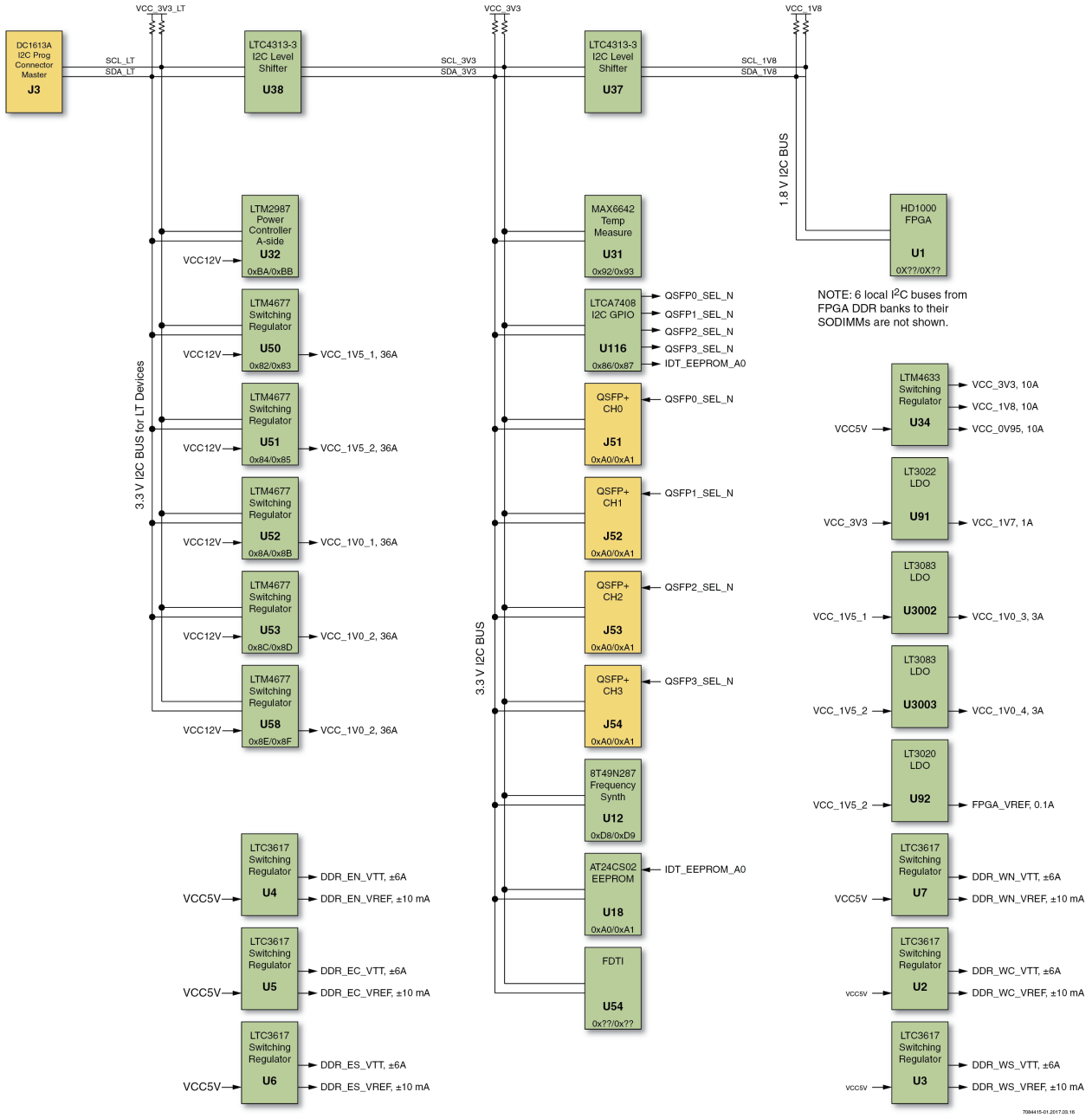

Figure Note

I^{2}C Address is 7 bits plus a read/write bit.

Figure 15: *Board Device, Power and I^{2}C Map*

Revision History

Version	Date	Description
1.0	March 20, 2017	• Initial Achronix release.
1.1	March 23, 2017	• Added I^2C Header (J3) Pin Connections (see page 31) table to the Miscellaneous Interfaces (see page 31) section • Fixed broken reference links