Achronix

Speedster7t FPGA
JESD204C IP Core

Key Core Features

The Achronix JESD204C IP core is designed for high-speed serial data links and supports:

- Up to 32 Gbps per lane
- Up to 8 lanes per link for scalable throughput
- Supports 64b/66b and 8b/10b encoding
- FEC, CRC 12, CRC 3, CMD data modes (64b/66b)
- Deterministic latency with system reference (SYSREF)
- Support for:
  - 1–256 multiblocks in an extended multiblock
  - 1–32 frames per multiframe (K)
  - 1–256 octets per frame (F)
- AXI-Lite configuration interface
- Additional support for:
  - Initial lane alignment
  - Scrambling
  - Character replacement
  - Error detection and link retraining
- Full backward compatibility with JESD204B

Core Deliverables

- Graphical configuration Interface in Achronix ACE
- Link Layer IP core design files in VHDL/Verilog
- Instantiation template
- Example designs
  - Hardware tested demo designs
  - Configuration scripts for VectorPath boards
  - Test bench and cases in VHDL
  - Expected simulation results delivered as log files
- Free evaluation IP core available for ACE

Applications

- Medical imaging
- 5G wireless infrastructure
- Test and measurement systems
- Aerospace and defense platforms
- High-speed data acquisition systems

High-Performance JESD204C IP

As demand for high-speed data converters (ADCs and DACs) continues to grow across 5G, test and measurement, medical imaging, and defense systems, designers need scalable, efficient, and deterministic data interfaces. To address these needs, the JESD204 interface standard was created — a high-speed serial communications standard that connects data converters (ADCs and DACs) to logic devices such as FPGAs, largely replacing older, bulky parallel LVDS interfaces used in the past. JESD204 gained widespread acceptance with the B revision and has since been upgraded with the release of the C revision. JESD204C enables higher bandwidth, improved link efficiency and greater flexibility.

Achronix offers a high-performance JESD204C IP core for Speedster®7t FPGAs, optimized for high-performance ADC and DAC interfaces while maintaining full backward compatibility with JESD204B. These capabilities make the core ideal for high-speed ADC/DAC interfaces, RF transceivers, and data acquisition platforms.

Backward Compatibility with JESD204B

Designers can seamlessly integrate legacy systems thanks to JESD204B backward compatibility. The IP supports both encoding schemes, enabling:

- Smooth system migration from JESD204B to JESD204C
- Mixed-generation converter support
- Reduced development risk

Optimized for High-Speed Converter Applications

The Achronix JESD204C IP supports key system requirements:

- Deterministic latency for synchronized systems
- Multi-lane alignment and synchronization
- Low overhead for maximum efficiency
- Flexible configuration (lanes, encoding, FEC, scrambling)

Speedster7t FPGAs — Natural Fit for JESD204C

The Speedster7t FPGA family is optimized for high-bandwidth workloads and eliminates the performance bottlenecks associated with traditional FPGAs. The combination of Achronix JESD204C IP with the Speedster7t FPGA architecture creates a powerful platform for high-speed converter systems.

High-Performance SerDes for JESD204C Connectivity

Speedster7t FPGAs integrate industry-leading 112 Gbps SerDes that deliver exceptional bandwidth, signal integrity, and low-latency performance. Supporting JESD204C data rates up to 32 Gbps, they provide robust, reliable connectivity to the latest high-speed ADCs and DACs, enabling next-generation data acquisition and signal processing systems.

2D Network-on-Chip for Data Movement

Unlike traditional FPGA architectures, Speedster7t features a 2D network-on-chip (NoC) that enables:

- High-bandwidth, low-latency data transport
- Efficient movement of JESD204 data streams across the device
- Reduced routing congestion and power consumption

This capability is critical for multi-channel JESD204 systems where data must be distributed quickly and efficiently.

Machine Learning Processors for Real-Time Processing

Integrated machine learning processors (MLPs) allow designers to:

- Perform real-time data analytics on converter outputs
- Implement DSP, filtering, and AI-based signal processing
- Reduce external processing requirements

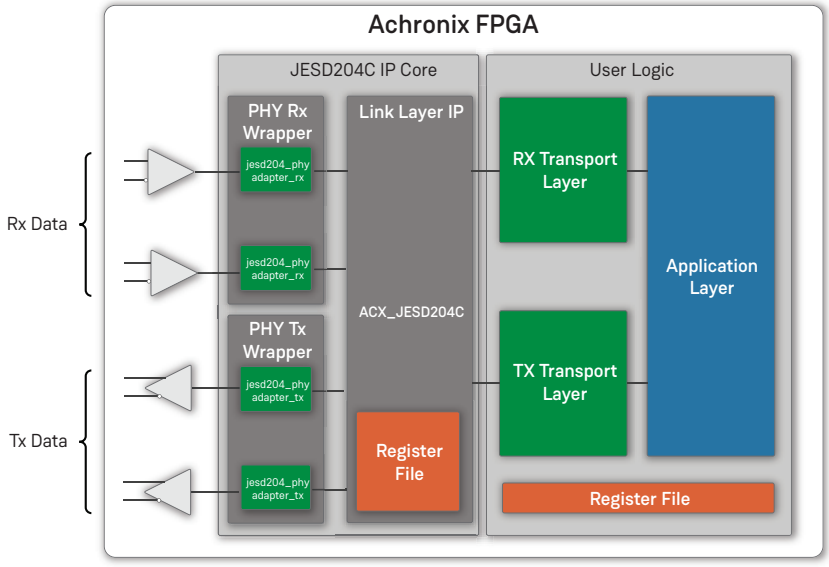
The array of embedded MLPs found in the architecture makes Speedster7t FPGAs ideal for edge processing applications such as radar, medical imaging, and 5G.

PCIe Gen5 Ports

A key feature of Speedester7t FPGAs that enables the movement of vast amount of data to and from the FPGA is the availability of up to two PCIe Gen5 interfaces. These two interfaces are part of the 2D NoC and deliver a combined bandwidth of 768 Gbps in one direction. Both interfaces can be configured as either Root Complex or Endpoint.

About Achronix Semiconductor Corporation

Achronix Semiconductor Corporation is a fabless semiconductor corporation based in Santa Clara, California, offering high-end FPGA-based data acceleration solutions, designed to address high-performance, compute-intensive and real-time processing applications. Achronix is the only supplier to have both high-performance, high-density standalone FPGAs and licensed eFPGA IP solutions. Achronix Speedster®7t FPGA and Speedcore™ eFPGA IP offerings are further enhanced by ready-to-use VectorPath® accelerator cards targeting AI, machine learning, networking and data center applications. All Achronix products are fully supported by the Achronix Tool Suite which enables customers to quickly develop their own custom applications.



JESD204C Core IP Block Diagram

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Achronix® Data Acceleration