achronix
SEMICONDUCTOR CORPORATION

PRODUCT BRIEF

HD1000 Development Kit

HD1000 DEV KIT HIGHLIGHTS

Development Board Features

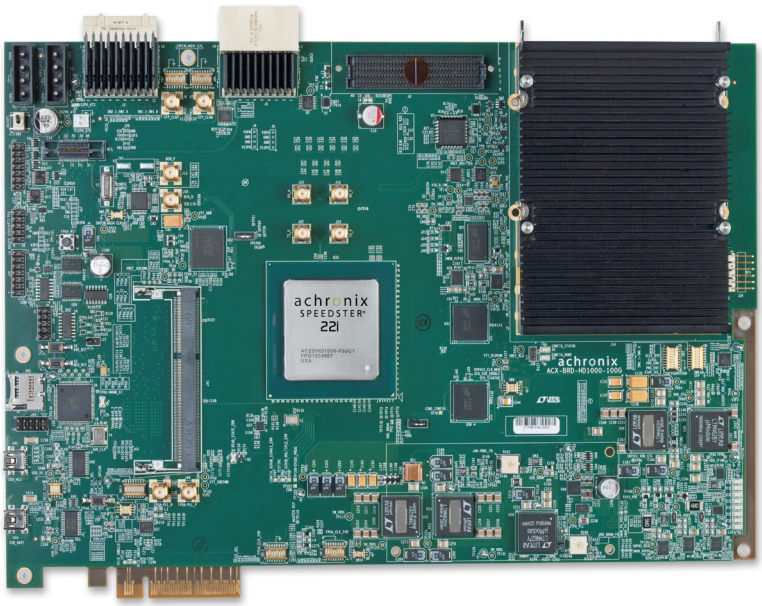
- HD1000 22-nm FPGA (see below for FPGA details)
- CFP cage for 100GE line interface
  - Adaptable to 2x40GE or 10x10GE
- Interlaken interface (AirMax connector pair)
  - 135Gbps to companion board/system
- PCI Express pluggable form factor
  - Gen 3 x8, for 64 Gbps throughput
- Access to a single SerDes lane via SMAs
- DDR3 module: Up to 4 GB (x64) at 1,866 Mbps
- Additional memories:
  - DDR3: 2Gb @ 933 MHz,
  - (2) RLDRAM3: 576Mb @ 933 MHz
  - 72Mb (x36) QDRII+ capable of up to 633 MHz
- FMC expansion port (HPC)
  - Ten SerDes lanes at 11.3 Gbps
  - Up to 160 signals (or 80 diff) at 1.6 Gbps
- Atmel Microcontroller for control and management
- Power supply modules
- Power on reset circuitry
- Oscillators/ crystals/ clock modules & synthesizers
- Power and temperature measurement
- JTAG interface
- SPI header for EEPROM access
- EEPROM for device configuration
- LEDs, switches, headers

HD1000 Device Features

- 1 million equivalent LUTs (700k LUTs + hardened IP)
- 86 Mbit on-chip memory (82 Mb BRAM, 4Mb LRAM)
- 756 28x28 multiply/accumulate blocks
- 960 programmable user IOs
- 64 SerDes lanes (1 to 12.75 Gbps)
- Hardened MACs: 100GE, 40GE, 10GE
- Hardened Interlaken ports: 135Gbps
- Hardened PCI Express Gen3 x8
- Hardened DDR3 controllers: six x72 at 1,866 Mbps
- Low power consumption
  - 22-nm Intel Tri-Gate transistor (low leakage)
  - Hardened IP

Included Accessories

- ACE Design Software
- Power Supply
- Bitporter Download cable



The Speedster22i HD1000 development kit from Achronix contains the world's first 22-nm programmable logic device — the HD1000, which is produced in Intel's 22-nm fabrication facility. The HD1000 development kit is optimized for development of networking and communication sub-systems — with 100 Gbps throughput, and offers the appropriate ports and memory capacity for these functions.

The HD1000 development kit enables evaluation of HD1000 fabric performance and hardened IP so you can quickly begin the evaluation and design process. You can exercise the full performance of the device, run prepared demos provided by Achronix and configure the device with your own design.

All fundamental HD1000 features are available — including programmable logic, RAMs, multiply/accumulate blocks, SerDes transceiver lanes, programmable I/Os and a rich collection of hardened IP. In addition to the HD1000 development board, the development Kit includes the ACE development tools, a Bitporter download pod and power supply.

High Bandwidth Throughput

Two distinct bidirectional datapath ports are provided. The "lineside" port features a CFP cage, which natively supports a single 100G Ethernet interface. With breakout adapters, this port can be flexibly reconfigured to support two 40GE ports or ten 10GE ports. The HD1000's on-chip hardened Ethernet MAC completes the lineside interface. On the "system" side, a 12x11.3Gbps Interlaken port is provided, in the form of a pair of AirMax connectors. This results in a convenient path to an external switch, network processor, or companion HD1000 Development board.

On-board Memory Features

The HD1000 development kit features extensive and varied memory support. The first level of memory support is the HD1000's on-chip memory, a total of 86Mb of SRAM - 82Mb of large 80Kbit BRAMs, and a further 4Mb of smaller distributed 640bit RAMs. Bulk external memory is provided in the form of a single-rank 2GB DDR3 module (supplied with the kit), operating at 933 MHz (1,866 Mbps). A dual-rank 4GB DDR3 module can also be used (not supplied). In the packet-based networking space, bulk external memory is typically used for packet buffering. Additional stand-alone memory devices include QDR2+, and RLDRAM3.

PCI Express, Expansion, and Other Features

The HD1000 development board is a PCI Express pluggable card, featuring a PCIe PCI-SIG compliant Gen3 x8 interface. Since the board receives power from dedicated power connectors, it can also operate in standalone mode. An FMC (HPC) connector is provided, enabling the addition of expansion circuitry or extra ports, such as ADCs, DACs,or video streaming.

A set of SMA connectors gives users access to a full bidirectional SerDes lane - for flexible use.

Design Methodology

The Achronix implementation flow uses an industry-standard RTL synthesis flow based on Synplify Pro from Synopsys. Working in conjunction with the synthesis tool, Achronix CAD Environment (ACE) provides placement, routing, timing analysis, bitstream generation, and FPGA configuration Simulation is supported using industry standard simulators, combined with onchip debug access allowing further verification capability.

Device Configuration

The HD1000 development board supports all programming modes available on the HD1000 FPGA. A standard JTAG interface can be used by the BitPorter Programming Pod to download designs directly into the FPGA. The BitPorter programming Pod (supplied as part of the Kit) can also be used to program the SPI flash, which is then in turn used to program the FPGA. The benefit of programming the SPI flash is that the configuration data is maintained between power cycles.

Summary

The HD1000 development board is the ideal platform for evaluation and product development for HD1000 based products — especially networking applications. Combining a flexible set of connectors with robust clock and power circuitry, the SDK enables fast, effective, and successful development programs using the most advanced FPGA available — the only 22-nm FPGA, and the only programmable device with such a rich hardened IP offering.

Ordering Information

Ordering Code: ACX-KIT-HD1000-100G

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