Achronix
bluespec

# Speedster7t FPGAs
# Bluespec RISC-V Cores

## Complete Hardware/Software Stack

### RISC-V Processor Soft IP

- Scalable and flexible processor
- Professionally implemented and verified
- Delivered as reference design
- Full source code

### Support for the Addition of Custom Instructions

- User-defined coprocessors to accelerate workloads
- Software-managed accelerators
- Supported via Bluespec's acceleration tools, Accelerate-HLS and Accelerate-HDL

### High-speed FPGA-based Hardware and Software Development Environment

- Packaged and tested by Bluespec
- Operating systems and toolchain provided
- Includes GCC, GDB, Open OCD

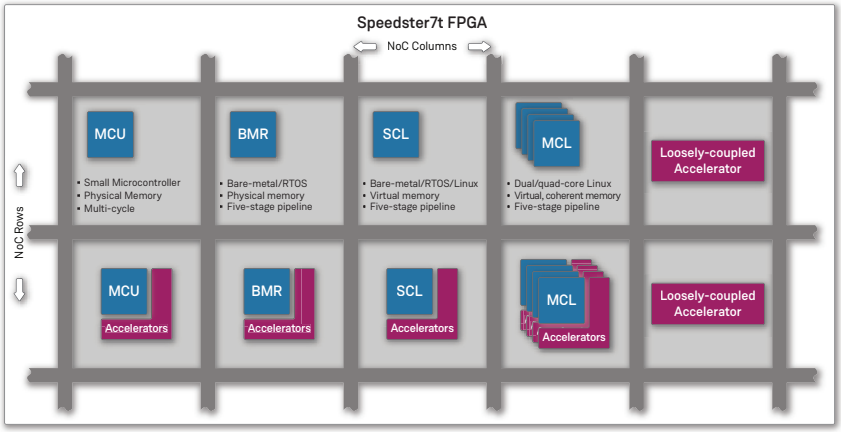
### Developed for, and Enabled on Achronix Technology

- 2D NoC enabled RISC V soft processor core
- Hardware-based development environment available with the VectorPath® Accelerator Card.
- Hardware/software reference design targeting the VectorPath card
- Hardware acceleration enabling tools
- A partner with RISC-V expertise

## Scalable Processing with Bluespec RISC-V Soft Processors

Bluespec, Inc., offers a portfolio of RISC-V processors provided as soft-IP for use in Achronix Speedster®7t FPGAs. Bluespec's processor offering ranges from a single RISC-V processor to multi-core RISC-V Linux processors featuring a five-stage processor subsystem that can run Linux out of the box on Achronix FPGAs. Bluespec's RISC-V processors also support custom instructions, enabling engineers to add accelerators managed through software to their Achronix FPGA designs.

The RISC-V processors are highly configurable and can be tailored to the user's application requirements, balancing performance with resources. These processing subsystems are built to take advantage of the scalability enabled by the Achronix 2D network on chip (2D NoC), which enables designers to incorporate one or more independent processor subsystems operating in a Speedster7t FPGA.




## Powered by Speedster7t FPGAs

The Speedster7t FPGA family is optimized for high-bandwidth workloads and eliminates the performance bottlenecks associated with traditional FPGAs. Built on the TSMC 7nm FinFET process, Speedster7t FPGAs feature a revolutionary new 2D NoC, an array of new machine learning processors (MLPs) optimized for high-bandwidth and artificial intelligence/machine learning (AI/ML) workloads, high-bandwidth GDDR6 interfaces, 400G Ethernet and PCI Express Gen5 ports. The 2D NoC connects all of the interfaces to over 80 access points in the FPGA fabric to deliver ASIC-level performance while retaining the full programmability of FPGAs.

## Target Applications

- AI/ML acceleration – Enables efficient processing of complex models and algorithms, crucial for AI-driven applications.
- Data center workloads – Provides customizable acceleration to enhance cloud computing, improving performance and efficiency in data processing tasks.
- Networking and communications – Facilitates high-speed data processing and advanced networking functionalities essential for robust communication systems.
- High-performance computing (HPC) – Supports demanding computational tasks in scientific research and simulations, offering scalability and high-speed processing capabilities.

## Benefits of Integrated RISC-V Soft Processors in Speedster7t FPGAs

### Efficient Processor Communication

The 2D NoC ensures high-bandwidth, low-latency communication between multiple RISC-V cores and accelerator functions hosted in the FPGA fabric. This communication is critical for applications that require coordinated processing across multiple cores, improving overall system performance.

### Scalable Multi-Core Architectures

With the 2D NoC facilitating efficient data movement, designers can quickly scale their RISC-V-based systems within the FPGA. More RISC-V cores can be added for the application without significantly increasing design complexity or compromising performance.

### Enhanced Data Processing Capabilities

The high bandwidth provided by the 2D NoC allows the RISC-V cores to quickly access large datasets from memory interfaces or external I/O, crucial for data-intensive applications such as machine learning inference, high-speed packet processing, and real-time analytics.

### Optimized Power Efficiency

The combination of Bluespec RISC-V cores and the 2D NoC leads to an overall reduction in power consumption. The efficient data routing minimizes unnecessary data movement and processing, ensuring that the FPGA operates efficiently, which is especially important for edge computing devices and applications with limited power resources.

### Simplified System Design And Integration

The architectural coherence between the 2D NoC and the RISC-V cores simplifies the system design process. Developers can focus on leveraging the computational capabilities of the RISC-V cores without worrying about the complexities of data routing and interconnect bandwidth, speeding up the development cycle and reducing time to market.

Contact Bluespec at sales@bluespec.com to learn more about Bluespec's RISC-V IP and tools!

| Feature | Details |
|---|---|
| Base architecture | RV32I or RV64I (integer) |
| CPU pipeline | Up to five-stage instruction pipeline |
| CPU FMAX | Up to 225 MHz |
| Coremarks | 1.72 Coremarks/MHz |
| Optional instruction extensions | · Multiplication (M)<br>· Atomic (A)<br>· Compressed (C)<br>· Single-precision floating point (F)<br>· Double-precision floating point (D) |
| Accelerators | Support for adding custom instructions/accelerators |
| Privilege level | User (U), supervisor (S), machine (M) |
| Operating system support | Complete RISC-V hardware/software stack (BareMetal, RTOS, or Linux) |
| CPU subsystem connections | 2D NoC, DDR, UART, debug port (optional), and GPIO |
| Peripheral extensions | Extension ports for user peripherals/hardware |
| Interrupt controller | Platform-level interrupt controller (PLIC) and core-level interrupt controller (CLINT) |
| Development tools | Packaged and tested open-source software tools |

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Achronix®
Data Acceleration