

## ViASIC's Place and Route Technology Chosen by Achronix Semiconductor

### Technology used as Place & Route functionality for Achronix CAD Environment

Research Triangle Park, N.C. - ViASIC Inc., an electronic design automation (EDA) company with breakthrough tools, IP and services for reconfigurable semiconductor fabrics, today announced that Achronix Semiconductor Corp. selected ViASIC's ViaPath™ place and route software for use in its Achronix CAD environment (ACE). ViASIC believes ViaPath is the only commercially available tool that can perform optimization, placement and routing for standard metal (one-mask or two-mask) programmable designs. The principles used in ViaPath are equally effective for structured ASICs and synchronous or asynchronous RAM-based FPGAs, resulting in a correct-by-construction finished IC design that meets all design closure requirements.

Achronix and ViASIC worked closely together to modify and integrate ViaPath's place and route code base for use in ACE. ACE is the Achronix design environment for its recently announced Speedster 1.5 GHz FPGA family.

According to Raymond Nijssen, chief software architect at Achronix Semiconductor, "To enable the world's fastest FPGAs we looked for an EDA partner we could rely on to deliver place and route capabilities as early as possible in our software development cycle. Our close collaboration in adapting the underlying engines and algorithms of ViaPath for Speedster has resulted in a powerful development tool. ViASIC exceeded our expectations."

Mark Goode, president and CEO of ViASIC, said, "We were honored to work hand-in-hand with Achronix as part of its development team and contribute our knowledge of configurable silicon products. And we were pleased to provide the P&R backbone that became an integral part of the Achronix software tool suite. We congratulate Achronix on its innovation in bringing the Speedster family to market, and feel proud to be a part of that effort."

### About ViASIC

ViASIC Inc. is the leading supplier of electronic design automation (EDA) tools, IP and services for reconfigurable semiconductor fabrics, both with and without SRAM. Reconfiguring far fewer metal layers than alternative approaches, ViASIC slashes design cost, time and risk. It enables ASSP providers, product designers, test chip designers, and other customers to reduce mask costs by up to 95% versus a standard ASIC design approach; it also speeds time to market by allowing manufacturing to begin before the design is fully completed, and by

allowing silicon debug much earlier in the design flow. Founded in 2000, ViASIC is headquartered in Durham N.C. For more information about ViASIC and its products and services, visit [www.viasic.com](http://www.viasic.com).

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