

Verific's Netlist-Only Parser Used in Achronix CAD Environment

Parser Used as Building Block for Speedster™ FPGA Development Software

Alameda, Calif. - Verific Design Automation today announced that Achronix Semiconductor Corporation, developer of the world's fastest field programmable gate array (FPGA) called Speedster™, uses Verific's Netlist-Only Parser in its Achronix CAD Environment (ACE).

Verific is best known for its Verilog, SystemVerilog and VHDL hardware description level (HDL) parsers and elaborators. Its Netlist-Only Parser includes a Verilog netlist reader and a generic hierarchical netlist database to help reduce development time for products operating at the gate level rather than the register transfer level (RTL).

The Achronix Speedster family of FPGAs delivers speeds up to 1.5 gigahertz (GHz), a three-fold increase in performance over traditional FPGAs. Achronix selected Verific's Netlist-Only Parser to speed time-to-market and because it provided fast Verilog and EDIF parsing, plus a complete extendable netlist data structure and netlist manipulation functions.

"Building ACE leveraging Verific's tool saved us a significant amount of time and effort," says Raymond Nijssen, chief software architect at Achronix Semiconductor. "Their industry-proven software and customer support enabled us to focus on developing our key software capabilities."

"Speedster is an amazing FPGA," remarks Michiel Ligthart, Verific's chief operating officer. "Being part of the development software that enables Speedster's disruptive lead in performance makes us proud of our own software."

As with all of Verific products, the Netlist-Only Parser is written in C++ and is shipped as source code.

About Verific Design Automation

Verific Design Automation, with offices in Alameda, Calif., and Kolkata, India, is a leading provider of Verilog and VHDL front-end software founded in 1999 by EDA industry veteran Rob Dekker. Verific's software is used worldwide in synthesis, simulation, formal verification, emulation, debugging, virtual prototyping, and design-for-test applications, which combined have shipped more than 40,000 copies. Corporate headquarters is located at: 1516 Oak Street, Suite 115, Alameda, Calif. 94501. Telephone: (510) 522-1555. Facsimile number: (510) 522-1553. Email: Email Contact. Website: www.verific.com.

Achronix and Speedster are trademarks of Achronix Semiconductor Corporation. All other brands, product names and marks are the property of their respective owners.