Speedster7t Power User Guide (UG087)

Speedster FPGAs

Preliminary Data

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Preliminary Data

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Chapter - 1: Power Supply Requirements

There are a number of different power supplies that are required for the Speedster®7t 7t1500 device as well as voltage tolerance levels for each of these supplies. This chapter provides details for the individual supplies and their tolerances. Also included are the connection guidelines for each of the power rails and recommendations for the power supply network sharing schemes at the board level.

The table below provides a list of power supplies used in Speedster7t FPGAs, the connection guidelines and tolerance levels for each of these supplies.

Table 1: ***Speedster7t FPGA Power Supplies***

Pin Name	Description			
Connection Guidelines	**Min Voltage (V)**	**Typ Voltage (V)**	**Max Voltage (V)**	**AC Ripple (mV pk-pk)**
CLKIO_<NE/NW/SE/SW>_VDDIO	**Clock I/O Analog Supply**			
The CLKIO power supply can be set to either of these supplies: 1.8V or 1.5V. The I/O standard can be configured at clock bank corner granularity (NW/NE/SW/SE). (1)	1.46	1.5	1.61	30
	1.75	1.8	1.93	30
CLKIO_<NE/NW/SE/SW>_VREF	**CLKIO Reference Voltage Supply**			
The reference voltage for the CLKIO can either be generated using a macro or can be driven by an external supply. If using an external supply, connect this pin to `CLKIO_*_VDDIO/2`	0.73	0.75	0.8	15
	0.87	0.9	0.96	15
CORE_VDD	**FPGA Fabric Power Supply Based On Selected Speed Grade**			
C1 – 0.90V	0.89	0.90	0.91	36
C2 – 0.85V	0.84	0.85	0.86	34
C3 – 0.75V	0.74	0.75	0.76	30
CORE_VDD_SENSE and VSS_SENSE				
These pins are used to monitor the CORE_VDD and VSS supplies at the die level and can be connected as feedback to the regulator for voltage correction. These pins can also be brought out as oscilloscope probe pins to monitor the die level ripples.	–	–	–	–
DDR4_S0_VAA	**DDR PLL Analog Supply**			
Connect to a 1.8V linear or low-noise switching power supply. (2, 5, 6)	1.78	1.8	1.82	36
DDR4_S0_VDDQ	**DDR4 PHY I/O Domain Power Supply**			
Connect to a 1.2V linear or low-noise switching power supply. (2, 5, 6)	1.16	1.2	1.24	38

Table 2: *Speedster7t FPGA Power Supplies (continued)*

Pin Name	Description			
Connection Guidelines	**Min Voltage (V)**	**Typ Voltage (V)**	**Max Voltage (V)**	**AC Ripple (mV pk-pk)**
ENOC_<N/NE/NW/S/SE/SW>_PLL_VDDA	**NoC PLLs Analog Supply**			
Dedicated power supply for each PLL. Requires an RC filtered 1.8V power supply from the board.	1.78	1.8	1.82	36
ENOC_<N/NE/NW/S/SE/SW>_PLL_VSSA	**NoC PLLs Ground Power Supply**			
Common ground supply for the peripheral NoC and GCG PLLs. (3)		0		
FUSE_VDD2	**eFUSE Module Analog Supply**			
Connect to a 1.8V linear or low-noise switching power supply.	1.78	1.8	1.82	36
FCU_VDDIO	**GPIO Associated with FCU/JTAG Analog Supply**			
Connect to a 1.8V power supply. This supply can be shared with CLKIO_*_VDDIO supply if a 1.8V standard is used for the CLKIO.	1.75	1.8	1.85	100
GCG_<NE/NW/SE/SW>_PLL_VDDA	**Clock Generator PLLs Analog Supply**			
Dedicated power supply for each PLL. Requires an RC filtered 1.8V power supply from the board.	1.78	1.8	1.82	36
GCG_<NE/NW/SE/SW>_PLL_VSSA	**Clock Generator PLLs Ground Power Supply**			
Common ground supply for the peripheral NoC and GCG PLLs. (3)		0		
GDDR6_<E/W>_VDDR	**GDDR6 PHY Digital Supply** – used for level shifting input signals from VDDR to VDDA domain and all output signals from VDDA to VDDR domain.			
Connect to a 0.85V supply. The GDDR6_VDDA supply can be shared with GDDR6_VDDR with a filter between them. (5, 6)	0.83	0.85	0.88	34
GDDR6_<E/W>_VDDA	**GDDR6 PHY Analog Power Supply** – used for digital logic, custom digital, data pipes and receive delay lines. Also used as analog circuit supply, clocking, global and local clock trees.			
Connect to a 0.85V supply. The GDDR6_VDDA supply can be shared with GDDR6_VDDR with a filter between them. (5, 6)	0.83	0.85	0.87	26
GDDR6_<E/W>_VDDIO	**GDDR6 I/O Power Supply**			
Connect to a 1.35V supply. The GDDR6_VDDIO supply can be shared with GDDR6_VDDP with a filter between them. (5, 6)	1.32	1.35	1.38	27
GDDR6_<E/W>_VDDP	**GDDR6 PHY PLL Supply**			
Connect to a 1.35V supply. The GDDR6_VDDIO supply can be shared with GDDR6_VDDP with a filter between them. (5, 6)	1.32	1.35	1.38	27

Table 3: *Speedster7t FPGA Power Supplies (continued)*

Pin Name	Description			
Connection Guidelines	**Min Voltage (V)**	**Typ Voltage (V)**	**Max Voltage (V)**	**AC Ripple (mV pk-pk)**
GPIO_<N0/S0>_VDDIO	**GPIO Analog Supply**			
The GPIO power supply can be set to one of these voltages: 1.8V, 1.5V, 1.35V,1.2V, or 1.1V. The I/O standard can be configured at corner granularity (NW/NE/SW/SE). (1)	1.07	1.1	1.14	30
	1.16	1.2	1.24	40
The GPIO power supply can be set to one of these voltages: 1.8V, 1.5V, 1.35V,1.2V, or 1.1V. The I/O standard can be configured at corner granularity (NW/NE/SW/SE). (1)	1.31	1.35	1.4	50
	1.45	1.5	1.55	60
	1.75	1.8	1.86	100
GPIO_<N0/S0>_VREF	**GPIO Reference Voltage Supply**			
The reference voltage for the GPIO can either be generated using a macro or can be driven by an external supply. If using an external supply, connect this pin to GPIO_*_VDDIO/2.	0.53	0.55	0.57	15
	0.58	0.6	0.62	20
	0.65	0.675	0.7	25
	0.73	0.75	0.78	30
	0.87	0.9	0.93	50
SRDS_N_PA_VDDH	**SerDes Analog High-power Supply**			
1.2V analog power supply for the SerDes. (4, 7)	1.16	1.2	1.3	10
SRDS_N_PA_VDDL	**SerDes Analog Low-power Supply**			
0.75V Analog power supply for the SerDes. (4, 7)	0.73	0.75	0.81	10
SRDS_N_PA_VSS	**SerDes Ground**			
Power supply ground for the SerDes lanes.		0		
TS_VDDA	**Temperature Sensor Analog Power Supply**			
Connect to a 1.8V power supply. This supply can be shared with the PLL_VDDA or FUSE_VDD2 power supply.	1.78	1.8	1.82	36
VCC	**Fabric Interface IP and NoC Digital Supply**			
0.85V digital power supply.	0.84	0.85	0.86	17

Table 4: *Speedster7t FPGA Power Supplies (continued)*

Pin Name	Description			
Connection Guidelines	**Min Voltage (V)**	**Typ Voltage (V)**	**Max Voltage (V)**	**AC Ripple (mV pk-pk)**
VSS	**Ground**			
All GND pins should be connected to the board's ground plane.		0		

Table Notes

1. Unused I/O banks should be powered — power balls should not be left floating or grounded.
2. The maximum supply ramp rate should be limited to 5 mV/µs.
3. PLL VSSA should not be shorted with any other VSS supply.
4. Connect these pins to a linear or low-noise switching power supply.
5. For any unused interface subsystems, the corresponding I/O should not be driven from any external source and should be left floating.
6. Even if the GDDR6 interface is not used, the corresponding power supplies need to be connected to the appropriate supplies.
7. If the DDR4 interface is not used, the corresponding power rails must be connected as follows:
   `DDR4_S0_VDDQ = GNDDDR4_S0_VAA = GNDDDR I/O` = Should be left floating. Do not connect to `GROUND` or `DDR4_S0_VDDQ` rail in PCB.
   The following DDR4 PHY interface signals are suggested to be connected as follows:
   Force `PwrOkIn` input to 0.
   Force `DFiClk/APBClk` inputs to 0 (If it is chosen to leave this clock running, extra power wastage is expected).
   Force Reset=1
   Force `PRESETn_APB=0`
   Force `WRSTN=0`
   Force `atpg_mode=0` (`atpg_*Clk` is don't care if `atpg_mode=0`).
8. The SerDes voltage pins should be connected to the appropriate supply even if the SerDes lanes are not used.

Chapter - 2: Power Supply Block Diagram

The diagram below represents a power sharing scheme for a use-case scenario that helps to reduce the required number of power supplies. The number can be further reduced depending upon the targeted speed grade of the device (see notes below). The sharing schemes are subject to change based on the requirements of the user design.

Guidelines on Power Sharing Schemes

- It is recommended that the PLL power supplies are not shared with the CLK/GPIO_*_VDDIO power supplies as the PLL is a low-noise supply with tight ripple specs. Also, imposing a tighter ripple spec (such as PLLs) on a more tolerable rail results in regulator overdesign. If this sharing is absolutely required, care should be taken to choose the right filtering scheme to ensure low-ripple noise on PLL power supplies. Also, simulations are a must to assess the noise with any filtering scheme.
- Each individual PLL also needs its own PLL_VDDA power supply filter to ensure low noise even though they can be adjacent on the package. This is required because the PLLs can generate significantly different frequencies which can cause interference.
- The TS_VDDA, FUSE_VDD and the DDR_S0_VAA supplies can be combined with the PLLs since these are low-current supplies and have the same ripple spec as that of the PLLs. Again, each of these supplies should also have their own filter.
- The FCU_VDDIO can be shared with CLKIO/GPIO_*_VDDIO supply if only a 1.8V standard is used for both the CLKIO and GPIO supplies and a stringent power supply ripple spec is met.

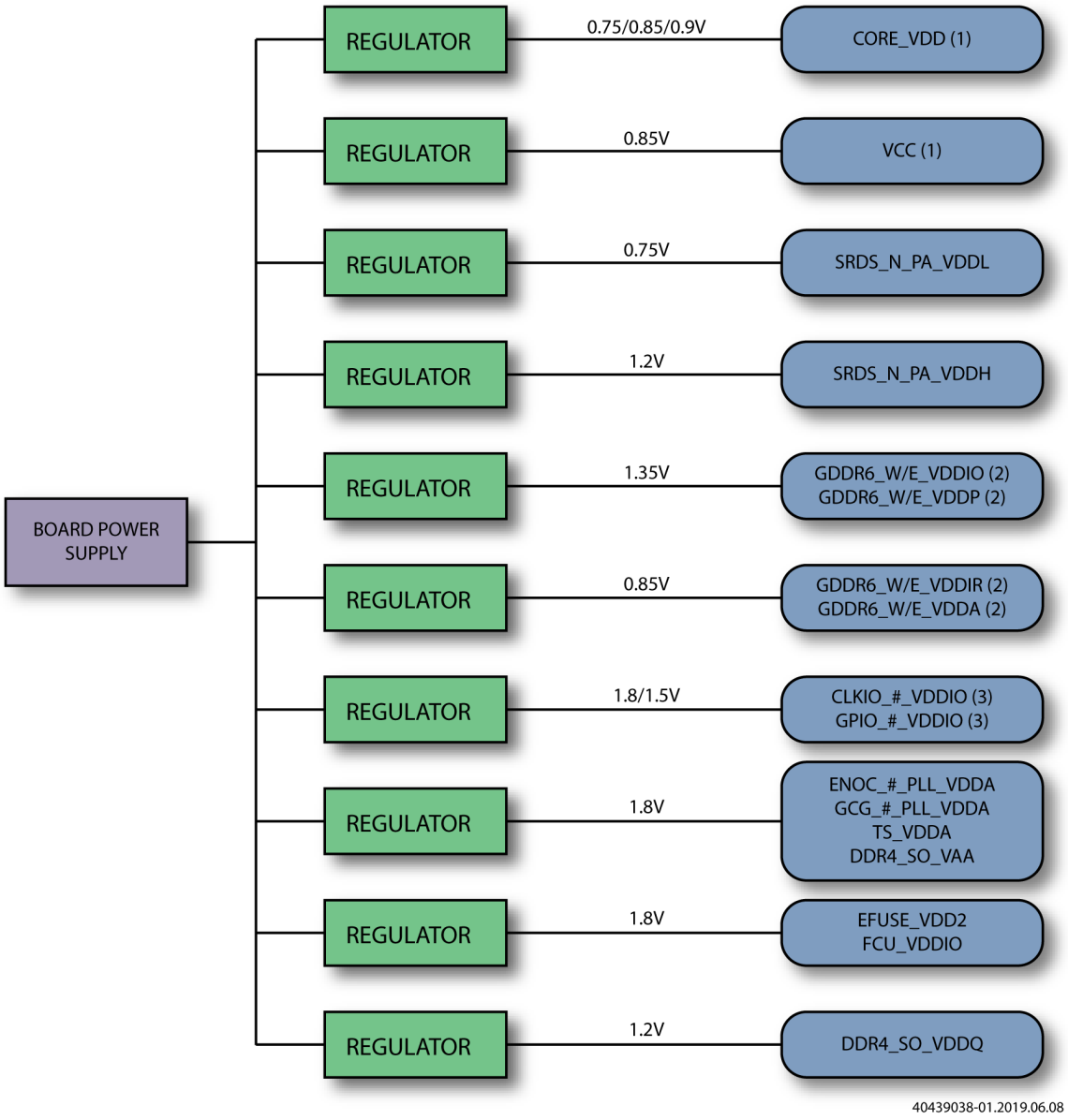

Figure 1: ***Speedster7t FPGA Power Supplies***

Figure Notes

1. The CORE_VDD and VCC supplies can be shared on the C2 speed-grade devices where the nominal voltages for these two rails are the same.
2. The GDDR6_W/E_VDDIO and GDDR6_W/E_VDDP supplies can be shared with a filter between them. Similarly, GDDR6_W/E_VDDR and GDDR6_W/E_VDDA supplies can be shared with a filter between them.
3. CLK_#_VDDIO and the GPIO_#_VDDIO can be shared, provided both I/O groups are configured to use 1.8V or 1.5V. If different power supplies are desired for each of the I/O groups, these supplies cannot be shared.

Chapter - 3: Power Sequencing

There is only a single power sequencing requirement applicable for the Speedster7t family of devices. The VCC power supply should be brought up before the EFUSE_VDD2 (1.8V) and pulled down after EFUSE2_VDD2 is pulled down. This sequencing is to ensure that there is no unwanted leakage when powering up the device.

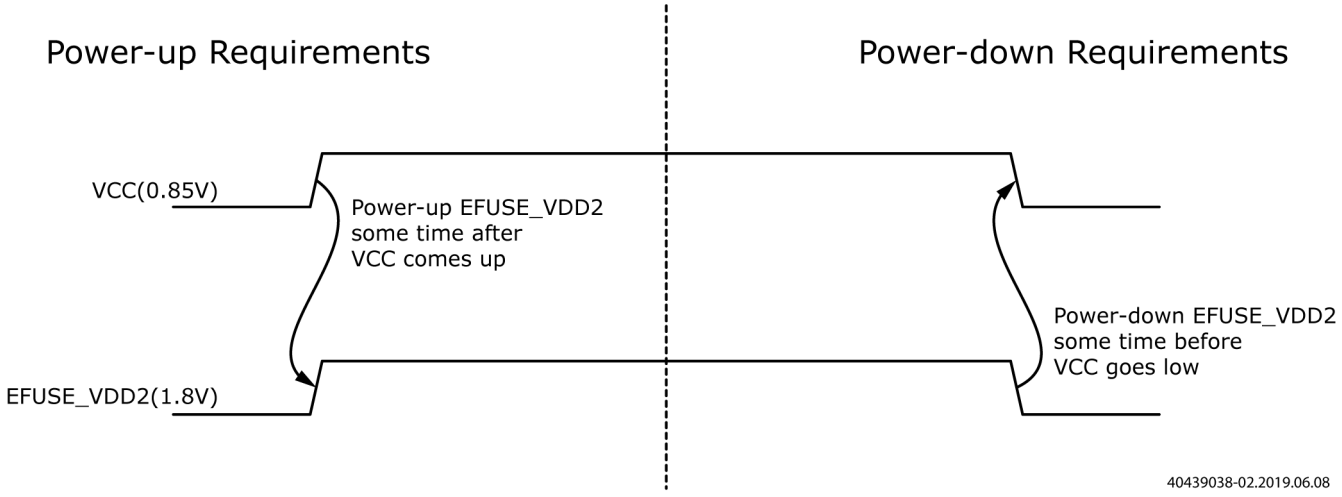

Figure 2: ***Speedster7t FPGA Power Sequencing***

Revision History

Version	Date	Description
1.0	27 Jun 2019	• Initial Achronix release.
1.1	26 Jan 2020	• Revised DC spec for SerDes, CLKIO and GPIO power supplies • Revised AC Ripple for GDDR_*_VDDA and CORE_VDD power supplies
1.2	30 Mar 2020	• Added description on supply connections when corresponding subsystems are not in use • Updated DC and AC ripple specs for CLKIO, GPIO ad FCU power supplies.
1.3	23 Sep 2020	• Added connectivity guidelines for the CORE_VDD_SENSE and VSS_SENSE pins
1.4	13 Apr 2021	• Updated connectivity guidelines for unused IP interfaces and SerDes power supply
1.5	11 Jan 2022	• Updated description for VCC supply