Speedcore ASIC Integration User Guide (UG064)

Speedcore eFPGA

Achronix®

Data Acceleration

Copyrights, Trademarks and Disclaimers

Copyright © 2021 Achronix Semiconductor Corporation. All rights reserved. Achronix, Speedcore, Speedster, and ACE are trademarks of Achronix Semiconductor Corporation in the U.S. and/or other countries All other trademarks are the property of their respective owners. All specifications subject to change without notice.

NOTICE of DISCLAIMER: The information given in this document is believed to be accurate and reliable. However, Achronix Semiconductor Corporation does not give any representations or warranties as to the completeness or accuracy of such information and shall have no liability for the use of the information contained herein. Achronix Semiconductor Corporation reserves the right to make changes to this document and the information contained herein at any time and without notice. All Achronix trademarks, registered trademarks, disclaimers and patents are listed at http://www.achronix.com/legal.

Achronix Semiconductor Corporation

2903 Bunker Hill Lane
Santa Clara, CA 95054
USA

Website: www.achronix.com
E-mail : info@achronix.com

Table of Contents

Chapter - 1: Introduction 5
Scope 5
Definition of Terms 5
Design Hierarchy 5
Responsible Engineer 5
Chapter - 2: Speedcore IP Integration Flow Overview 6
Performed at the Architectural Stage by the Architect 6
Performed by the ASIC Integrator 6
Performed by ACE Users 6
Chapter - 3: Speedcore Front-end (RTL) Integration and Simulation 7
Fabric Architecture 7
Speedcore I/O Pins 10
I/O Pin Nomenclature 10
Pin Selection and Connection Overview 12
Pin Selection Process 12
Pin Selection Guidelines 12
Speedcore IP Simulation 13
Full-Chip Simulation Overview and Deliverables 13
Full-Chip Simulation Flow with End-User Design 15
Chapter - 4: Speedcore Static Timing Analysis 23
Speedcore Interface Timing Modes and Clocking Scenarios 23
Functional Simple Timing Mode (STM) 23
Functional Advanced Timing Mode (ATM) 24
DFT Timing Mode 25
User Interface Clocking Scenarios 25
Achronix Supported Procedure 28
Speedcore ASIC Timing Closure Methodology 28
Speedcore Timing Abstraction Methodology 28
How to Handle Speedcore I/O and Timing Modes 29
Clock Related Timing Considerations 30
Speedcore Timing Corners and Margins 33

PVT and RC Corners 33
STA Margins 34
Speedcore Boundary SDC Generation for use by ACE 35
Timing Analysis Procedure 35
SDC Generator 35
SoC STA Modes 36
SDC Verification 36
Examples of Data and Clocking Scenarios, and Related SDC Constraints 36
SoC Timing Constraints Definition Recommendations 59
Chapter - 5: Speedcore Physical Design Integration 60
Floorplan Placement Guidelines 60
Aligning Power/Ground Routes to the Speedcore Instance 60
Aligning the Speedcore Instance to Signal Pin Routing Grid 60
Placement of Logic Blocks Around the Speedcore Instance 60
Revision History 62

Protected Document

The full contents of this document are confidential and require a signed non-disclosure agreement (NDA) between Achronix and your company. Talk with your Achronix sales representative about obtaining an NDA.

Gaining access to Achronix confidential design documents requires the following steps:

1. Ensure that your company/organization has an active NDA with Achronix.
2. Log into your Achronix support portal account. If you do not yet have a support portal account, please refer to "How Do I Register for an Achronix Support Account" to register and set up your account.
3. When logged in, click the link "Submit a request" located next to your user name.
4. Select **Document Request** under Submit a request.

5. When the ticket form is selected, a number of ticket fields are revealed. Enter a description of the document(s) you are wanting to access, and click **Submit** when complete.
6. A support engineer will review your request and, if approved, will grant you access to the documents/files.

> **Note**
>
> The fields, Subject and Description are not meaningful for the process, but are nevertheless required to submit the ticket.