Evaluating Speedcore IP For Your ASIC

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Introduction

By exploiting Achronix Speedcore™ embedded FPGA (eFPGA) IP — IP proven in multiple ASIC designs for wireless, datacenter and high-performance computing (HPC) applications — designers of SoCs can now add logic programmability to their solution, resulting in a single ASIC that can adapt to many applications. While many system architects may already have strong ideas on how an eFPGA core could add value to their ASIC/SoC design even before having formulated a specific application, it may not be clear how to start an evaluation. Often the question foremost on a potential customer's mind is "How can I assess Speedcore IP's ability to solve my problem?"

Achronix refers to this pre-engagement stage as phase zero — an evaluation period where customers formulate application ideas and test them using tools and models. This paper presents a walk-through of phase zero, providing guidelines to customers who want to explore and refine ideas for employing a Speedcore eFPGA in their SoC.

Why Embed Speedcore eFPGA?

System designers encounter a broad variety of processing problems which are inadequately addressed by embedded CPUs, GPUs or generic discrete FPGAs. The primary motivation for SoC design teams to explore eFPGAs is to find technology that can solve problems which they have found to be either intractable or can only be patched at a high cost, often with considerable difficulty.

In addition to the inherent system-level advantages of embedding a programmable hardware accelerator in an SoC (see the Achronix white paper *Embedded FPGA – a New System-Level Programming Paradigm* (WP006)), Speedcore eFPGA IP provides other advantages to SoC designers. By foregoing the use of a discrete FPGA and embedding programmable logic functionality as a personalized combination of LUT, memory and DSP blocks, Speedcore eFPGAs offer fundamental improvements in signal delays, bandwidth, latency, power and cost. Board design becomes simpler while power and cooling requirements are significantly reduced. Finally, the system BoM is improved from both a cost and component count standpoint as the discrete FPGA along with all its supporting devices (level shifters, voltage regulators, bypass capacitors, and so forth) are eliminated.

Getting Started

The first step for customers in an evaluation is to begin acquiring a feel for Speedcore IP via the design process. By developing designs using the Achronix ACE design tools, customers can familiarize themselves with the Speedcore design flow as well as the resources available to support their design efforts. This familiarization step helps to clarify customer design ideas for Speedcore IP in their ASIC and sets expectations for performance and power consumption.

Phase zero quickly evolves into a highly collaborative environment. IP and design flow training, Q&A sessions and application discussions. This interaction implicitly calls for the sharing of documentation, tools, expertise and detailed technical information. As a consequence, a mutual nondisclosure agreement (NDA) is needed between Achronix and the customer to protect everyone's intellectual property rights. After completion of the NDA, Achronix delivers login credentials to the evaluators for them to download the ACE design tools and obtain an evaluation license.

ACE includes an Achronix-optimized version of Synopsys Synplify Pro and full support for Speedcore IP, including two example instances that can be targeted for design evaluation. These example instances differ in size and resource counts (LUTs, BRAM and so forth) to permit the ASIC design team to compile their designs into a Speedcore eFPGA that fits their requirements.

ACE design tools also offer multiple reports on performance, resource utilization and power consumption, as well as tools for layout, place and route, bitstream generation, debug support, static timing analysis and both functional and timing-annotated simulation. ACE is a best-in-class software design tool that stands with the best FPGA tool capabilities in the industry. Moreover, the Achronix applications team is available to provide training and support in conjunction with an ACE evaluation licenses.

Sizing a Speedcore Instance

Utilizing the ACE design tools, a customer can benchmark Speedcore IP by synthesizing RTL targeting either of the two generic Speedcore examples. This process is often executed with the assistance of the Achronix applications team.

During this benchmarking, the evaluators typically collate resource usage (LUT, DFF, BRAM, LRAM, DSP64 and ALU), F_{max} and early power consumption profiles. With this data, the customer can assess the resources needed for their particular Speedcore instance. Achronix then provides details for the Speedcore instantiation that accommodates the customer's requirements, including projected die size and aspect ratio of the IP, static power profile, configuration time and mix of programmable blocks. Variables which influence these early size assessments of a Speedcore instance include the designs themselves, customer tradeoffs between performance and power consumption, as well as a customer's target process node and metal stack.

Some Common Issues

It is not unusual for customers to start with RTL that previously targeted a discrete FPGA. Such code is often already optimized for a particular FPGA vendor's architecture. To retarget such code for Speedcore eFPGA, there is an IP library available in ACE that helps with the conversion from Xilinx and Intel/Altera primitives to Achronix primitives.

There are always hardware differences between different FPGA products. For example, Speedcore eFPGAs have a 4-input LUT, which is different from the 6-input LUT architectures from other FPGA companies. Using a 4-input LUT over a 6 input was a deliberate architectural choice for Speedcore eFPGA, as empirical data indicates 4-input LUTs provide the optimal performance with respect to silicon area for the great majority of programmable logic applications.

Another important difference is Speedcore support for distributed memory. Speedcore eFPGAs have logic RAM (LRAM) blocks that are 4,096-bit, configured as 128 × 32. Speedcore LRAM is larger than distributed memory arrangements of other competitors' offerings, yet smaller than block RAM architectures, making Speedcore LRAM ideal for midsize applications such as buffering tasks. Speedcore LRAM has proven to be particularly suited for a variety of networking and multimedia functions, including applications in packet management and video processing. By offering both block RAM (BRAMs) and industry-leading LRAMs, Speedcore memory blocks help designers select the right memory configuration to optimize performance per square millimeter of silicon for their personalized Speedcore instance.

Attributes for inferencing BRAMs, DSP or other functions are supported by the ACE design tools. If a design calls out attributes specific to a discrete FPGA architecture, designers simply need to change the name to the appropriate Speedcore attribute.

Any RTL originally intended for standard cell implementation will work for targeting Speedcore eFPGAs, but will benefit from efforts to optimize the code for the Speedcore architecture. To this end, customers can review the application note, *Coding Guidelines for Speedcore eFPGAs* (AN003), which offers a set of best practices for crafting code that will more efficiently utilize Speedcore logic, memory and DSP resources.

The Achronix Applications team often becomes deeply involved in such issues with Speedcore customers. This involvement is a normal part of the collaborative evaluation effort between Achronix and ASIC teams, and is especially helpful for interpreting design results to drive further improvements in power consumption, compile times, configuration times and performance.

Business Engagement

Upon completion of phase zero, all that remains to move the design forward is the completion of a licensing agreement between Achronix and the customer. The parameters of such an agreement (terms, conditions, duration and so forth) are substantially like those for licenses for embedded CPUs, standards-based circuit blocks and most other embedded IP in the semiconductor industry.

From this point on, Achronix and the ASIC design team can move forward jointly with the standard methodology for designing and integrating Speedcore IP into a custom ASIC design. There are four phases to the Speedcore methodology. In each phase, various files are provided at key points of the ASIC design flow — some from the ACE design tools, others directly from Achronix — to facilitate integration of a Speedcore instance into the overall ASIC architecture. The methodology is described in depth by the white paper, *Speedcore General Methodology Overview*, provided to all Speedcore licensees.

Conclusion

Phase zero is the beginning of a Speedcore design and how you begin matters. From a technical perspective, you will want to explore the possibilities to maximize the benefit of having your ASIC deployed with a Speedcore instance with a mix of resources well suited to your current and future programmed configurations. Achronix will help you along this road, providing support, training and feedback in employing tools, benchmarking designs and dealing with optimization issues.

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