5G Advanced and 6G Evolution Powered by FPGA Technology

White Paper

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Executive Summary

5G, 5G Advanced, and 6G bring many technical and commercial challenges that need to be met if the promised benefits of this new cellular technology are to be truly achieved. Any solution in this space must deal with the evolving specifications — FPGA and eFPGA IP technology is critical to the successful deployment of these next-generation network technologies.

5GA and 6G Market Background

Clearly, 5G is now much more than just the next cellular technology for handset connectivity. 5G and the evolution of cellular connectivity to 5G Advanced and 6G, enables multiple new use cases and creates new opportunities for new stakeholders, who previously did not have cellular connectivity as part of their product mix.

Today, 5G cellular technology extends beyond telecoms, providing connectivity for a variety of other use cases such as industrial IoT, automotive, and smart city. Work on 5G and the evolution of the standards to 5G Advanced and 6G enables the connection of billions of new devices and a variety of other sensors in homes, cities, and factories, supporting convergence with IT technologies, and general replacement of tethered, wireline connectivity.

5G infrastructure deployments are continuing to ramp up significantly faster than that of 4G, with mobile network operators (MNOs) rolling out 5G to reach more than one billion subscribers two years ahead of where it took 4G to achieve similar levels.

A comprehensive evaluation of the 5G technology and market and the applicability of Achronix technology is covered in the Achronix white paper, *Enabling the Next Generation of 5G Platforms* (WP029).

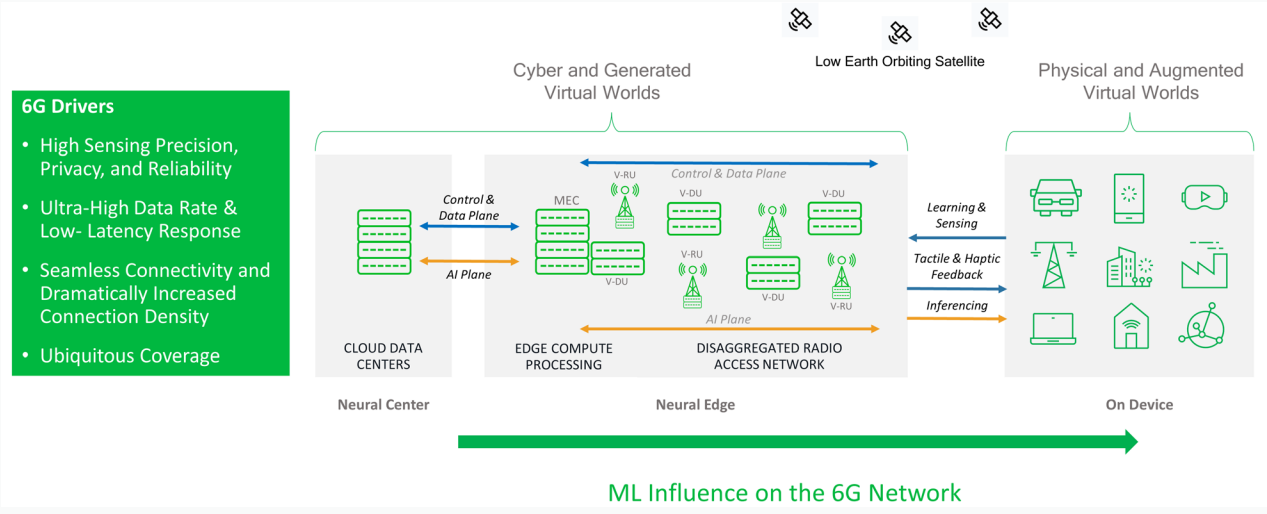

Figure 1 – ***5G Advanced and 6G Network Infrastructure Challenge: Network; ML Influence on the 6G Network***

We are about to enter the realm of 5G Advanced with work on 3GPP Releases 18 through 20 already well underway. It is through these releases that many of the baseline capabilities required for 6G will start to be realized, leading to the fleshing out of the architecture to meet the initial 6G requirements and eventually to support equipment development and technology evaluations.

The convergence between the radio access network (RAN) and the core network (collectively referred to a RAN-Core) will increasingly see edge compute and RAN capability being co-located at the neural edge. This convergence will see hyperscalers such as Meta, Microsoft, and Amazon start to target their cloud products at the RAN edge.

The air interface will become much more complex with more bandwidth being allocated at higher spectrum ranges. This transition will necessitate higher levels of vector processing in the radio and beam-steering technology being adopted to service efficient utilization of this bandwidth.

The disaggregation of the RAN will continue into 6G. Machine learning will play a much more important part as the network itself interprets and decides where workloads should run according to traffic load, latency, and security criteria. In addition to the usual control and data planes running through the network, it is expected that a specific AI plane will be introduced across the network for the management of machine learning tasks and related decision-making.

6G workloads will be run in distributed pools of virtualized baseband capability (or virtualized distributed units, v-DUs) that will be tightly synchronized allowing network operators to dynamically provision their network to meet changing workloads.

Radio units will be connected through front-haul links that dramatically scale capacity from today's deployment. 100 or even 400 Gbps links may be needed to carry the traffic from the v-DUs to the radio units in 6G.

Achronix can capitalize on all these challenges with our FPGA technology and offer a platform that is not only scalable in terms of performance but can offer designers the flexibility to adapt to changes as these manifest themselves through the specifications process over the next decade.

Achronix Use Cases and Advantages in the 5G Advanced and 6G Markets

The key to meeting these challenges is the selection of the appropriate architecture to meet the needs of algorithmic acceleration, connectivity, and security processing. Customers need solutions that can scale to meet the expected exponential increase in performance of the L1 interface and for the addition of ML processing that is expected in RAN management.

Achronix can meet these challenges with our architecture and technology. Through a process of functional validation, physical validation, and physical implementation, Achronix can ensure designers select the optimal level of performance in a form that meets their requirements.

The figure below illustrates some of the ways in which Achronix technology can be utilized in designs for 5G and 6G, representing how standalone Speedster FPGAs and Speedcore eFPGA IP technology can be utilized. In the future, Achronix believes that FPGA technology in chiplet form can also be used in heterogeneous multi-chip module (MCM) SoCs along with other memory and CPU chiplets.

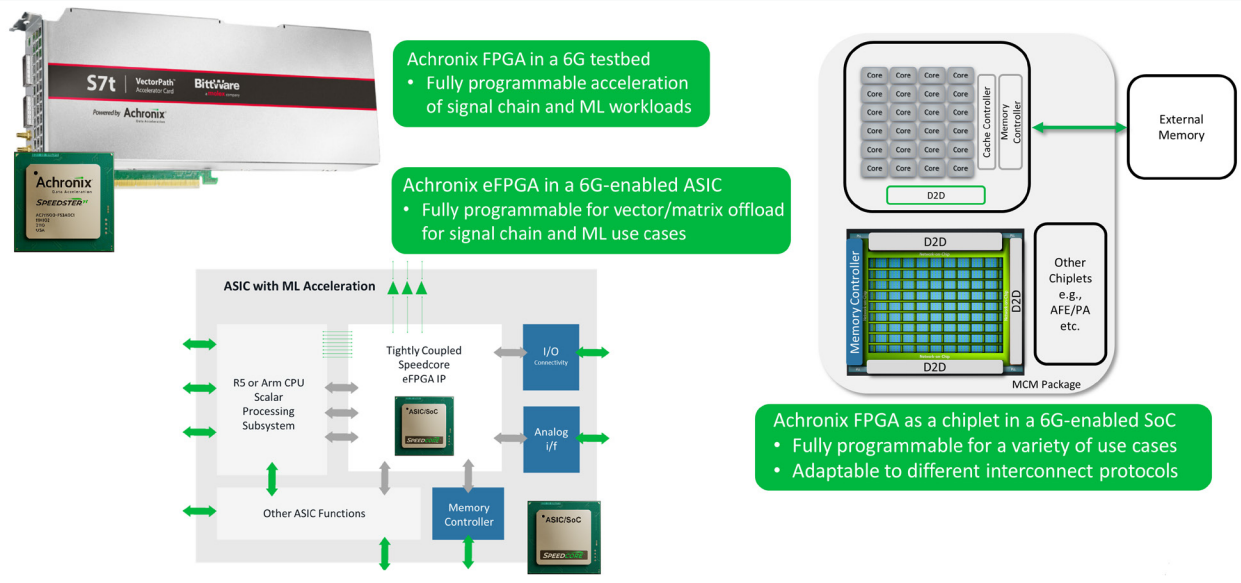

Figure 2 – ***FPGA/eFPGA Targets for 5G Advanced and 6G Workload Acceleration***

Achronix is already successfully engaged in helping several customers meet their 5G requirements with a mix of its FPGA and eFPGA IP technology. Our continued development of the technology and alignment with several specialist partners enable us to assist customers to include algorithmic processing for radio processing, radio connectivity, and security as well as integrating machine learning capability into their designs. The technology will not only allow developers to meet initial specification requirements but will allow them to future-proof designs capable of scaling to support future enhancements to the cellular specifications when designs are deployed in the field.

FPGA can be Considered for the Acceleration of Cellular Workloads

The opportunity offered by the 5G Advanced and 6G markets can be both met with standalone FPGAs based on the Speedster7t family but also with Speedcore eFPGA IP. In the case of Speedcore IP, Tier 1 OEMs can utilize eFPGA instances or a variety of SoC acceleration capabilities.

Achronix has developed a series of reference implementations that illustrate the value of our technology. These reference implementations are being developed in cooperation with several partners with specific and in-depth knowledge of cellular algorithms and technology that can be implemented on our FPGAs for specific needs (for example, air interface processing, interface connectivity, and machine learning technologies).

The VectorPath acceleration card offers an excellent platform for developers to evaluate our technology and support low-volume test deployments.

FPGA or eFPGA-based Designs can be Used in the Following Platforms

The following use cases represent examples of where Achronix solutions are already gaining traction:

5G SoC ASIC

Achronix eFPGA technology has been used for algorithmic acceleration in radio and base-band designs. These designs utilize Achronix Speedcore eFPGA IP technology in ASICs for a variety of algorithmic acceleration and connectivity tasks. The Achronix designs supported highly performant designs to offload certain functions of the ASIC while offering flexibility in the customer's ASIC designs. This flexibility helps customer designs adapt to evolving standards throughout the product's lifecycle.

6G Testbed

Achronix FPGA technology is ideal for the development of 6G future connectivity and algorithmic development capability (see figure below). The Achronix FPGA-based solution is uniquely positioned to support a combination of the performance and scalability required for 6G development work. A VectorPath accelerator card platform can be used to host development work targeting the Speedster7t AC7t1500, providing the I/O capacity in terms of radio connectivity with multiple 400 Gigabit Ethernet interfaces together with an interface to virtualized containerized workloads running on CPU blades in a chassis mount system.

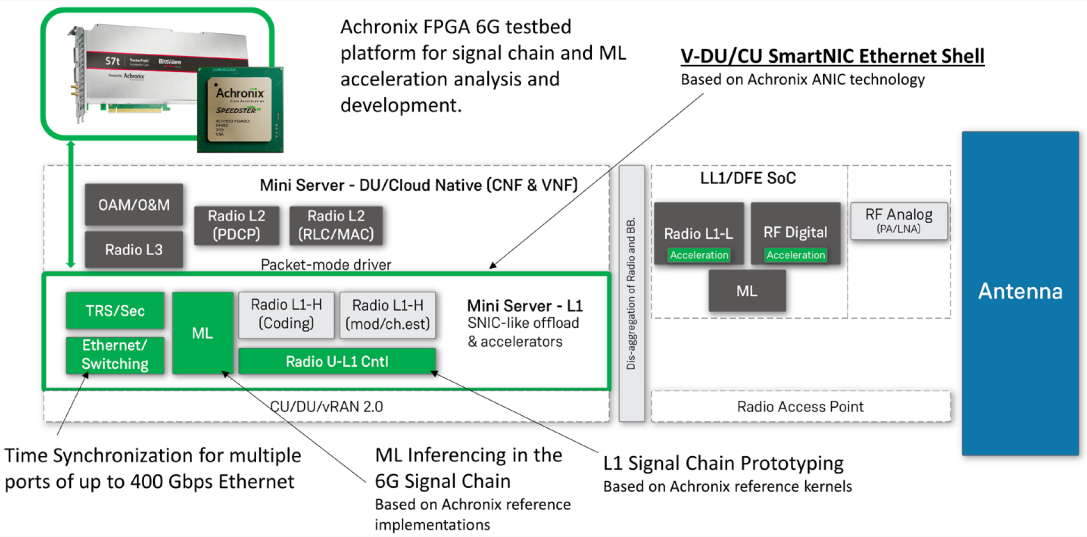

Figure 3 – ***Achronix Reference PoC for 6G Testbed***

Unique to the Speedster7t architecture are machine learning processor (MLP) blocks embedded within the FPGA fabric which provide significant additional processing power to run their vector processing algorithms for L1 radio processing. The MLPs also provide the ability to run machine learning algorithms closely coupled with the L1 air interface design.

This platform utilizes the Achronix Network Infrastructure Code (ANIC) Ethernet shell IP as the baseline for any 6G development and can be used with baseline 5G kernels written for our vector engine by one of our partners to jump start development work. Once development is complete the Vectorpath accelerator card can be deployed as a 6G testbed design in MNO networks in low volumes to demonstrate their 6G technology.

Using FPGAs to Gain a Competitive Advantage in 5G and 6G Designs

There are several technology options available for the acceleration of 5G and 6G workloads. Scalar processing on CPUs is a baseline technology choice for SoC designs because of the programming flexibility offered for handling workloads. For workload acceleration, GPUs, DSPs, ASICs, and FPGAs are all options that require consideration.

FPGAs offer the best blend of the capability to accelerate and offload workloads from CPU subsystems, and that the mix of our FPGA and eFPGA IP fabric combined with 2D NoC and MLP architecture offers designers optimum performance and flexibility. The choice of technology will be influenced by a mix of:

- Workload flexibility and the ability to adapt the design to meet changes in algorithms as the standards evolve
- Latency and how each of the technologies may meet specific latency criteria
- Determinism
- Power efficiency

Solutions are likely to mix several technologies in a single device or platform using MCMs and various new system packaging technologies to integrate several functions as chiplets into a heterogeneous architecture. Achronix is well-positioned to be able to meet these challenges with its FPGA and eFPGA IP technology.

The Competitive Advantage Provided by Achronix FPGA Technology

Interesting challenges emerge as designers start to consider how they can handle these new 5G Advanced and 6G radio and network workloads. The graph in this figure below considers the performance requirements for 6G radio processing.

- Technical studies for 6G starting now
- 6G will require much higher capacity/complexity than 5G
  - E.g., sub-THz spectrum 100 GHz to 300 GHz
- AI/ML powered E2E networks – coupling with the signal processing chain
- Network splitting and radio will necessitate diverse equipment and SoC choice
- Drives SoC technology evolution:
  - Software driven versus acceleration offload
  - Heterogeneous and monolithic integration
  - MCM, mixed analog and digital SoC technology

▪ ***One size cannot fit all. Solutions needed to handle different scenarios efficiently.***

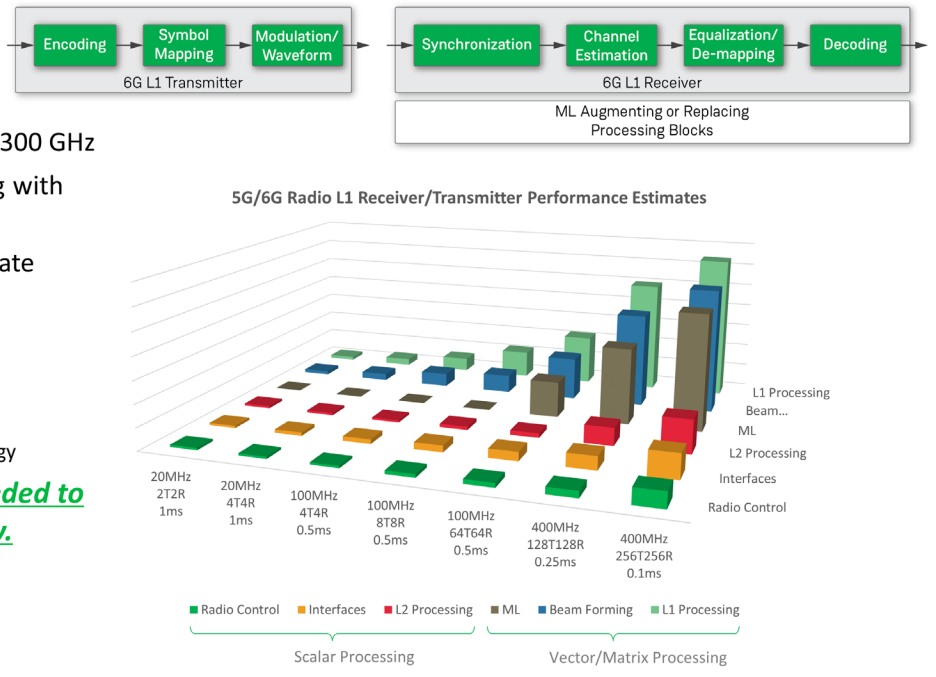

Figure 4 – ***5G Advanced and 6G Network Infrastructure Challenge: Radio & Network Hierarchy***

Looking at the processing requirements for the air interface for the 5G Advanced and 6G transmitter and receiver, for example, there is roughly a 10-fold increase in performance for the L1 processing and for beamforming in 6G. The same is true for machine learning workloads. The brown columns again grow exponentially through the various releases to 6G. Machine learning as a technology is likely to be focused on solving three main challenges in the radio:

- For channel coding, deep learning will reduce the time complexity of channel coding without deterioration of performance.
- For massive MIMO, deep learning models such as convolutional neural networks are likely to improve the bit error rate performance and system capacity while optimizing channel estimation and feedback.
- Non-orthogonal multiple access in the radio interface, along with massive MIMO, will deliver enhanced performance and a reduction of internal power consumption to increase energy efficiency.

These dramatic increases in performance required for certain 5G Advanced and 6G workloads are likely to heavily influence the choice of acceleration offload solution. The combination of the Achronix FPGA fabric, appropriately dimensioned I/O interfaces, hard vector processing engines (such as MLPs), and hard 2D NoC in the Speedster7t family allows designers to access exactly the level of acceleration performance required to meet these exponential increases in combined L1 air interface and machine learning algorithms associated with efficient radio resource management.

Just as we are likely to see the emergence of innovative technologies to support the combination of vector and scalar processing then how these are physically implemented is likely to change also. Heterogeneous architectures utilizing MCM technology where blocks of eFPGA IP are co-located with CPUs and

memory chiplets integrated into the same package mixing analog and digital technologies are likely to be a common solution. Achronix meets this challenge with the ability to offer a common scalable architecture between standalone Speedster7t FPGA and Speedcore eFPGA technologies. In the future, it is likely that many of the heterogeneous SoC-based solutions will be based on an MCM approach.

The choice of technology source and the choice of whether to design ASICs, and MCMs internally or to license ASSP designs with the eFPGA integrated is key — Achronix, as an independent company, can support the entire range of solutions.

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